

National Exams May 2003

98-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made with the answer of the question.
2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination,
3. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.
4. Each question carries 25 marks and marks for each question part are indicated in brackets.
5. All questions are of equal marks. Total marks = 100
6. This paper contains **Six (6)** questions and comprises **NINE (9)** pages.
7. Data on some relevant Digital ICs is provided in the Appendix.

1. (a) The circuit shown in Figure Q1 is designed for a simple digital combination lock with three binary inputs (A, B, C) and an active low output $\overline{\text{UNLOCK}}$. The circuit is supposed to generate the output signal for a unique input combination only. Verify the correctness of the circuit. Does it generate the $\overline{\text{UNLOCK}}$ signal for a unique input combination?

(10 marks)

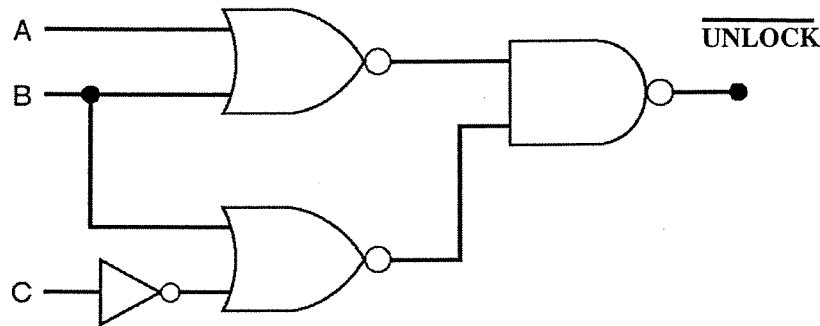


Figure Q1

- (b) Simplify the switching function, F by using Karnaugh-map method.

$$F(A, B, C, D) = \sum m(1, 3, 4, 5, 6, 7, 9, 10, 11, 15)$$

(15 marks)

- (i) Draw the K-map for the function and find all the prime implicants.
- (ii) Identify essential prime implicants.
- (iii) Write the simplified Boolean expression.

2. (a) Define the following terms with respect to digital devices.

(8 marks)

- (i) Fan-out
- (ii) $I_{IL}(\text{max})$
- (iii) Speed-power product
- (iv) Noise margin

- (b) A 74LS04 inverter is to be used to drive one input each of OR (74LS32), AND (74HC08) and NOR (74LS02) gates and both inputs of a NAND (74S00) gate.

(17 marks)

Question No. 2 continues on Page 3

- (i) Draw the circuit and indicate the flow of currents when the inverter has a LOW output.
- (ii) Why are the values $I_{IL}(\max)$ and $I_{OH}(\max)$ specified as negative in Table Q2?
- (iii) Using the specifications provided in Table Q2, determine whether there will be total voltage and current compatibility. Justify your answers.

Table Q2

Parameter	74HCT	74HC	74LS	74S
$V_{IH}(\min)$	2.0 V	3.5 V	2.0 V	2.0 V
$V_{IL}(\max)$	0.8 V	1.0 V	0.8 V	0.8 V
$V_{OH}(\min)$	4.9 V	4.9 V	2.7 V	2.7 V
$V_{OL}(\max)$	0.1 V	0.1 V	0.5 V	0.5 V
$I_{IH}(\max)$	1 μ A	1 μ A	20 μ A	50 μ A
$I_{IL}(\max)$	-1 μ A	-1 μ A	-0.4 mA	-2 mA
$I_{OH}(\max)$	-4 mA	-4 mA	-0.4 mA	-1 mA
$I_{OL}(\max)$	4 mA	4 mA	8 mA	20 mA

3. (a) Identify any advantages and disadvantages of BCD numbers. (4 marks)
- (b) Design a BCD validity circuit that detects invalid BCD numbers from any given 4-bit number. The output of the validity circuit is LOW when it detects an invalid BCD number. Construct the truth table and produce simplified Boolean expression using Boolean algebra. Implement the simplified Boolean expression by using NOR gates only. (14 marks)
- (c) Implement the combinational logic circuit developed in part (b) by using a PAL16L8 diagram given in the Appendix. Show the intact PAL fuses by crossing them in the diagram. You may attach the duly completed PAL16L8 diagram to your answer book. (7 marks)

4. (a) Study the D-type flip-flop circuit of Figure Q4 as given below with three inputs L, I and C.

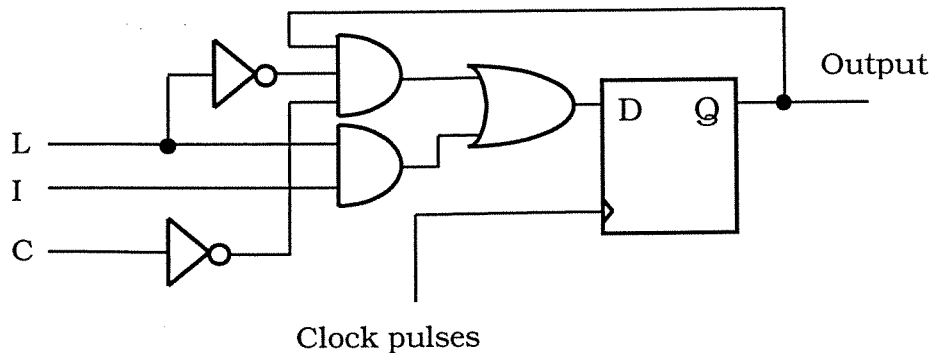


Figure Q4

Determine the output, Q at positive clock transitions for all the combinations of inputs.

(9 marks)

- (b) Design a sequence controller that simulates the traffic light. The controller has three active-LOW (TTL) outputs that drive green, yellow and red LEDs respectively. The LEDs emulate the following traffic light sequence repeatedly:
- Green LED on for 3 seconds
 - Yellow LED on for 1 second
 - Red LED on for 3 seconds

In the case of an out-of-order sequence, the controller must restart from the green LED within eight clock pulses.

Design the controller using a suitable size ring counter and some logic gates. Assume that a TTL clock signal of 1Hz is available.

(16 marks)

5. (a) Consider a 4-bit ripple up-counter that is driven by a 20-MHz clock. Each flip-flop of the counter has a propagation delay of 20 nsecs.

(15 marks)

- (i) Determine the maximum clock frequency, f_{\max} that can be used with this counter without missing any counter state.

Question No. 5 continues on Page 5

- (ii) Find the counter states, if any that will not occur due to propagation delays.
- (iii) What will be the maximum frequency, f_{\max} if the counter is expanded to 5-bits?

(b) A J-K flip-flop circuit is shown in Figure Q5.

(10 marks)

- (i) Determine the frequency of the output signal for a clock input of 1.5 MHz.
- (ii) Using a D-type flip-flop, design a circuit that performs the same function.

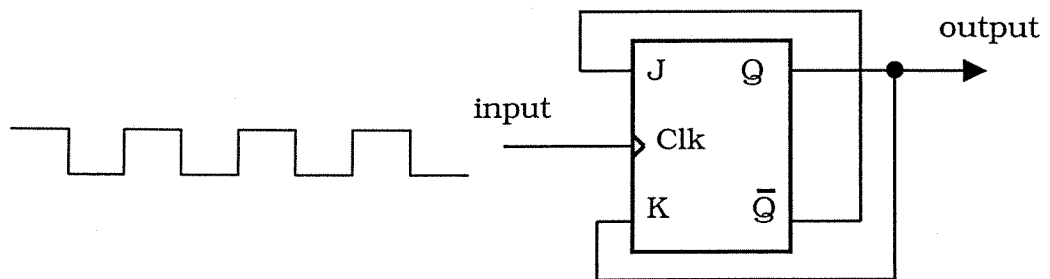


Figure Q5

6. Develop a parallel-to-serial converter sequential circuit that converts 6-bit ($D_0:5$) binary numbers into serial output when the enable signal, EN is high. The block diagram of the circuit is shown in Figure Q6(a). Each data input bit is represented at the serial output (logic 1 or 0) for $1\mu\text{sec}$ duration and the serial output remains at logic 0 when the circuit is not enabled. The circuit should insert two additional logic 1 bits to the serial output data one as a start bit while the other as a stop bit. Figure Q6(b) shows a typical serial output for $(011010)_2$ data after inserting start and stop bits.

The converter sequential circuit may consist of logic gates, flip-flops, counter (e.g. 7493 or 74293) and MUX (e.g. 74151). Assume that a 2MHz TTL clock is also available.

(25 marks)

Figures Q6(a) and Q6(b) are on Page 6

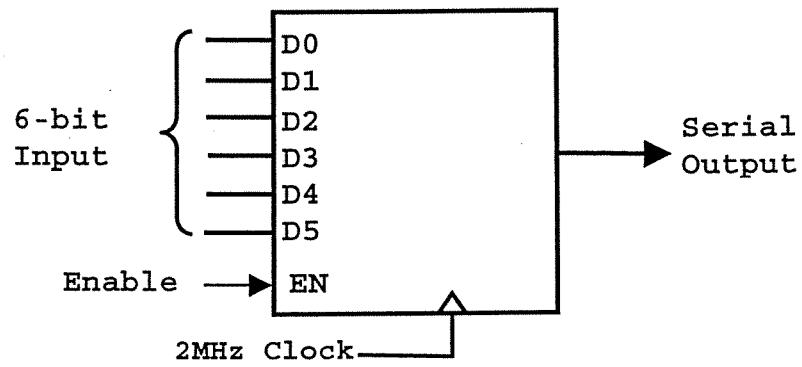


Figure Q6(a)

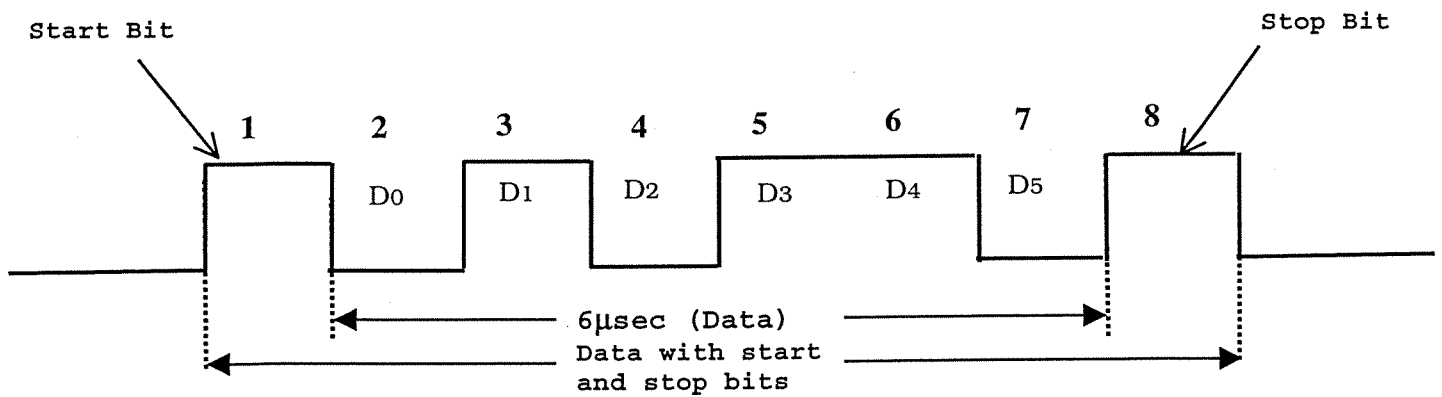
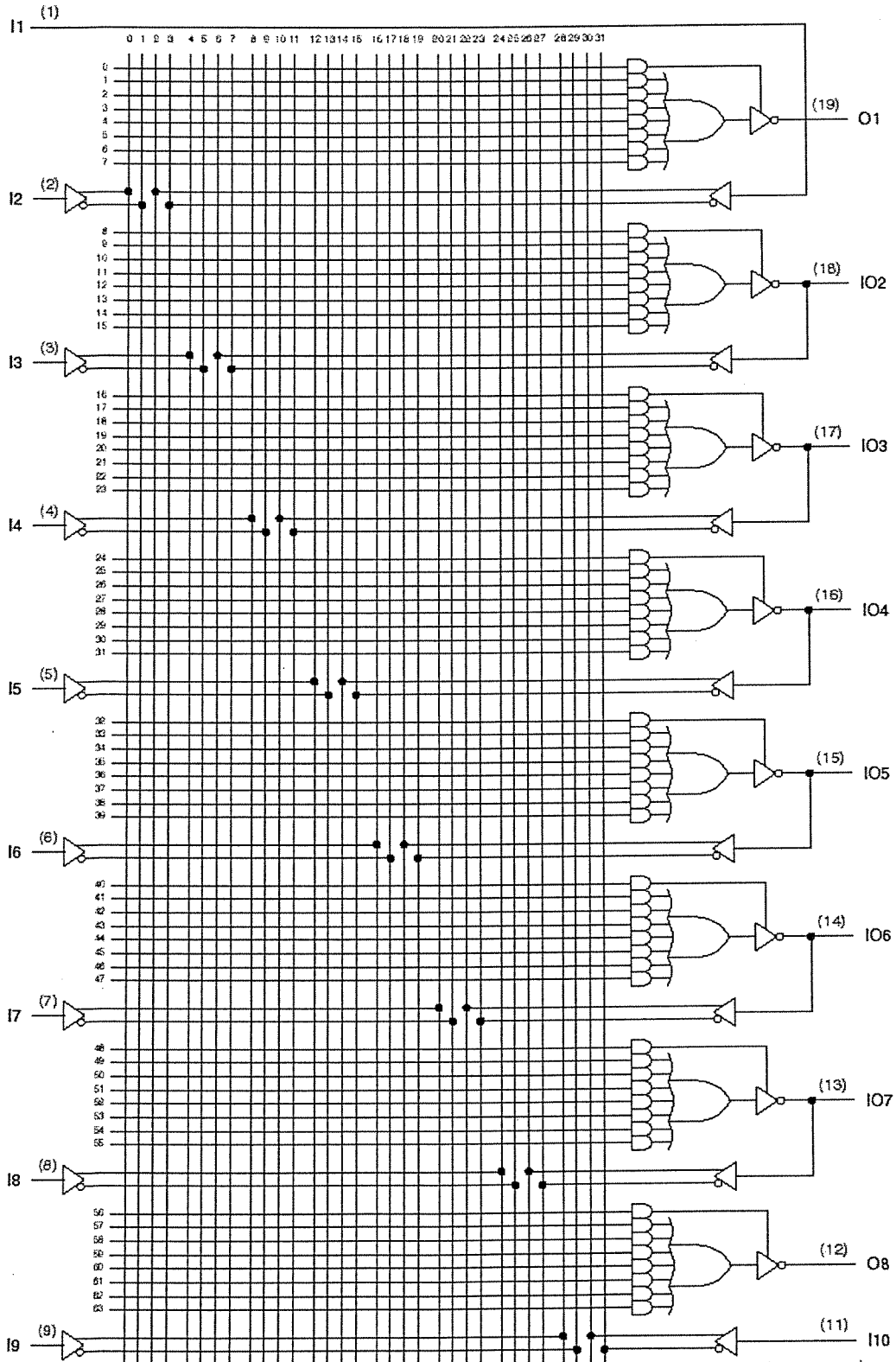


Figure Q6(b): Serial output for (011010)₂ 6-bit binary data

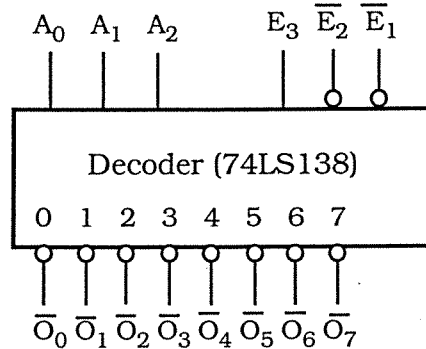
APPENDIX

PAL16L8



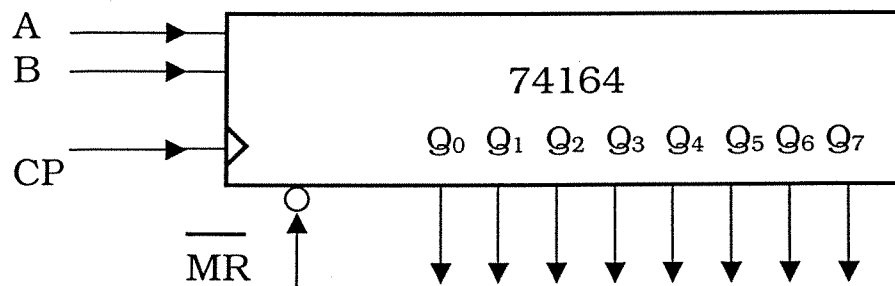
Decoder, Counter, MUX and Shift Register Data Sheets

74LS138: 3-to-8 Decoder



Inputs			Outputs
$\overline{E_1}$	$\overline{E_2}$	E_3	
0	0	1	Respond to input code $A_2A_1A_0$
1	x	x	Disabled - all HIGH
x	1	x	Disabled - all HIGH
x	x	0	Disabled - all HIGH

74164 A 8-bit Shift Register



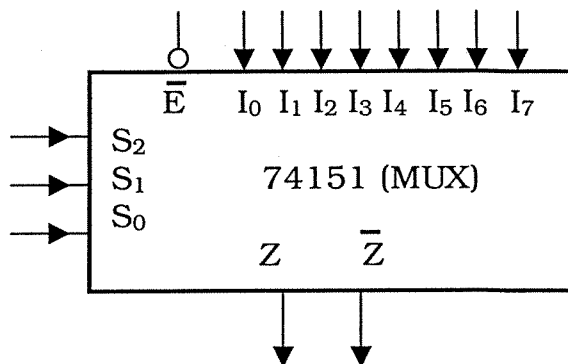
- An eight-bit shift register with all FF outputs Q_0 , Q_1 , Q_2 , Q_3 , Q_4 , Q_5 , Q_6 and Q_7 are externally available.
- Inputs A and B are ANDED together to produce the serial input to flip-flop Q_0 .
- Shift operation occurs at PGTs of the clock input CP.
- The \overline{MR} input resets all FFs asynchronously on a LOW level.

74151 8-to-1 Multiplexer

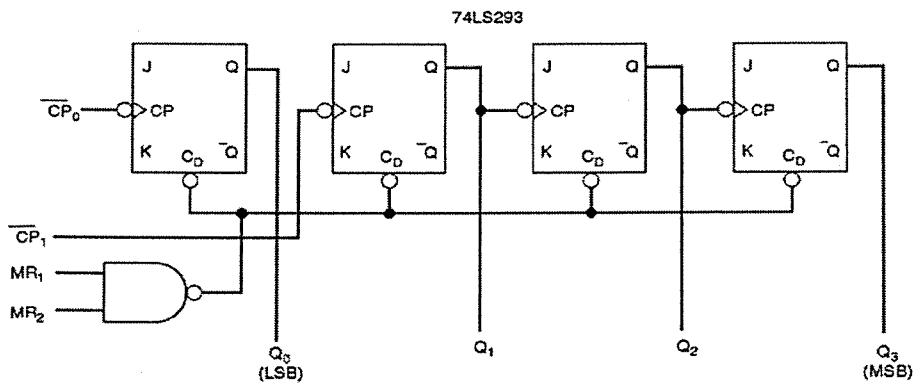
Inputs

Outputs

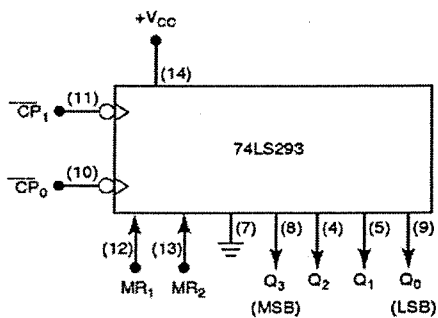
\bar{E}	S_2	S_1	S_0	Z	\bar{Z}
H	X	X	X	H	L
L	L	L	L	\bar{I}_0	I_0
L	L	L	H	\bar{I}_1	I_1
L	L	H	L	\bar{I}_2	I_2
L	L	H	H	\bar{I}_3	I_3
L	H	L	L	\bar{I}_4	I_4
L	H	L	H	\bar{I}_5	I_5
L	H	H	L	\bar{I}_6	I_6
L	H	H	H	\bar{I}_7	I_7



74293 : 3/4-bit counter



*All J, K inputs are internally connected HIGH.



^(b) End of Paper