

**National Exam May, 2002**  
**92 Comp A-2** (SOFT-AG)

**Digital Systems Design**

**3 Hour Duration**

**Notes:**

This exam has 5 pages and 5 questions. Make sure you have a complete copy.

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made.
2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a Closed Book Exam.
3. Any **FOUR (4) questions** constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.
4. All questions are of equal value.

**Question 1 (25 Marks)**

You are to design a synchronous sequential circuit that has a single one-bit input  $x$  and a single one-bit output  $z$ . In any clock interval, the output  $z$  is to be a 1 provided that the current input  $x$  is 0 **and** that in the previous four clock intervals the inputs were 1,0,1,0. At all other times the output  $z$  is to be 0. A possible input sequence and the corresponding output sequence is as follows:

$$\begin{array}{r} x = 1 \quad 1 \quad 0 \quad 1 \quad 0 \quad 0 \quad 0 \quad 1 \quad 0 \quad 1 \quad 1 \quad 0 \quad 1 \quad 0 \quad 0 \\ z = 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1 \dots \end{array}$$

Use D flip-flops and standard logic gates to realize your design. Your design should use the smallest number of states and gates. Give a state transition diagram, and clearly identify your state assignment. Give a state table, perform state reduction as necessary and demonstrate that no further reduction is possible. Give a transition table and show that no lockout will occur in your design. Illustrate your design with a logic diagram.

**Question 2 (25 Marks)**

- a) (5 Marks) Draw a block diagram of a PLA showing the major components and provide a description of its operation. How is the size of a PLA specified? Under what conditions would one decide to use a PLA as opposed to a ROM for an application?
- b) (20 Marks) Derive the program table for a minimum-size PLA that generates the product of two unsigned 2-bit binary numbers  $A_1A_0$  and  $B_1B_0$ . Note that  $A_1$  and  $B_1$  are the most significant bits and  $A_0$  and  $B_0$  are the least significant bits.

**Question 3 (25 Marks)**

Binary numbers between 0 and 7, 3-bits only for each number, are received serially on an input line  $x$ . The bits are synchronized with a clock and arrive with the **least significant bit first**. For example the number 3 (011) would be received in three successive clock cycles with  $x=1$  in the first clock cycle,  $x=1$  in the second clock cycle, and  $x=0$  in the third clock cycle.

Design a sequential circuit to detect when the input binary number is greater than 2 and less than 7. Starting from a reset state with  $z=0$ , the circuit will have an output  $z=1$  during the clock cycle immediately following that in which the third bit was received for a binary number representing 3, 4, 5, or 6. At all other times, the output  $z$  is to be 0. The output is to remain at the logic 1 level for only a single clock cycle and then return to zero. A possible input and output sequence is as follows:

$x =$	1	0	0	1	0	0	1	1	0	1	0	1	1	1	0
$z =$	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0

Your design should use the smallest number of states and gates. Use D flip-flops in your implementation, and analyze your design to ensure proper operation. Give a state transition diagram, and clearly identify your state assignment. Give a state table, perform state reduction as necessary and demonstrate that no further reduction is possible. Give a transition table and show that no lockout will occur in your design. Illustrate your design with a logic diagram.

**Question 4 (25 Marks)**

Select a microprocessor of your choice for this question (for example from the Intel 80X86 or Motorola 680X0 families, or other). You **must** select a processor that has a data bus at least 32 bits wide and an address bus at least 32 bits wide and allows byte (8-bit), word (16-bit) and long word (32-bit) access to memory. Complete the following questions:

- a) Describe the address and data bus structures for this processor. Describe the essential control bus signals that are available for this processor.
- b) Describe the memory organization for this processor. How are 8-bit wide memory banks defined in terms of address assignment and data bus connections? Does this processor support Big Endian or Little Endian data transfers/storage and what do these terms mean? Does this processor have any restrictions on storage/access of 16-bit words or 32-bit long words at specific addresses in memory?
- c) Describe the memory read and memory write bus cycles for this processor. You may wish to illustrate your discussion with representative timing diagrams. Clearly describe the nature and use of control signals needed to complete the data transfer in these cycles.
- d) Design a section of memory for this microprocessor that provides 2Mbytes of SRAM that is byte, word, and long word addressable. This section of memory must have the first byte located at a start address of 30000000 hexadecimal, and occupies sequential addresses that increase from this starting address. You must use 128K by 8-bit SRAM chips. Each SRAM chip has 17 address pins, 8 bi-directional data pins, an active low output enable pin  $OE^*$ , an active low write enable pin  $WE^*$ , and an active low chip select pin  $CS^*$ . The SRAM chip is enabled when  $CS^*=0$  and is disabled when  $CS^*=1$ . A read from the chip occurs when  $CS^*=0$  and  $OE^*=0$ . A write to the chip occurs when  $CS^*=0$  and  $WE^*=0$ . Your design must ensure that  $CS^*=0$  with  $WE^*=0$  and  $OE^*=0$  cannot occur at the same time. Your design must not produce bus conflicts for addresses outside of the range for this memory segment. Assume that 2-to-4 and 3-to-8 line decoders (as and if required) and any standard logic gates are available for your design. You do not need to show every wire in your design. Organize the derivation and presentation of your solution to show the overall structure, using buses if desired, in sufficient detail that another engineer could understand your design. You do not need to consider any timing properties of the design.

**Question 5 (25 Marks)**

Select a specific microprocessor family or microprocessor device. For example, you may select the Intel 80XXX family, or a specific 80XXX microprocessor, or the Motorola 68XXX family, or a specific 68XXX microprocessor, but your selection is not limited to these. Choose a family or device that is well documented, widely used in North America, and that supports external memory and input/output, and also supports vectored interrupts and direct memory access.

Describe this microprocessor family or device, using diagrams and point-form descriptions wherever feasible, by addressing the following major points labeled a) through e). Each of these major points carries a five-mark weight and exhaustive detail is not required. Possible subpoints are listed under each major point as a guide. Organize your discussion to give a logical presentation that another engineer familiar with general microprocessor concepts could understand.

- a) **(5 Marks) *Internal Architecture and Bus Structure:*** Briefly describe the internal structure of the microprocessor(s). What is the programmer's model including register structure? What addressing schemes are supported? Describe the address, data, and control buses.
- b) **(5 Marks) *Memory Architecture:*** What memory architectures are supported by the microprocessor(s)? What memory sizes and data widths are supported? How is synchronization with slow memory devices implemented? How are data of width greater than one byte stored, byte by byte, in terms of a typical memory map for these systems?
- c) **(5 Marks) *Input/Output (I/O) Structure:*** What I/O architectures are supported by the microprocessor(s)? How is synchronization with slow I/O devices implemented?
- d) **(5 Marks) *Interrupts:*** How are vectored interrupts handled within the microprocessor(s)? Describe how the interrupt service routine operates. Contrast interrupts to polled I/O for this architecture.
- e) **(5 Marks) *Direct Memory Access DMA:*** How is DMA supported by the microprocessor(s)? Describe the logical sequence of operations that occur in order to execute DMA on this bus structure. What modes of DMA transfer are supported?

**End of Exam**