

PROFESSIONAL ENGINEERS ONTARIO
NATIONAL EXAMS DECEMBER 2002
98-COMP-A3 (COMPUTER ARCHITECTURE)

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made;
2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a **Closed-Book** exam;
3. Any **EIGHT (8)** questions constitute a complete paper and only the first eight questions that you answer will be marked;
4. All questions are of equal value (12.5 marks).

NAME (Please Print) :

SIGNATURE :

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Question [1]
Question [2]
Question [3]
Question [4]
Question [5]
Question [6]
Question [7]
Question [8]
Question [9]
Question [10]
TOTAL

- a) Draw a simple block diagram of the Von-Neumann architecture and describe, very briefly, the operation of the computer.
- b) In an M-stage pipelined Arithmetic Logic Unit (ALU), the throughput could be increased by up to a factor M (Compared to a non-pipeline ALU). What are the conditions that should be satisfied in order to achieve this maximum performance?
- c) What are the advantages of using an Input Output Processor (IOP) instead of an interrupt-based programmed IO?

Question [2]

Computer Structure and Typical Processor Architecture

{12.5 marks}

a) List the main advantages and disadvantages of the Harvard Architecture?

b) What are the main features of Micro-Controllers compared to General Purpose processors?

c) Describe, very briefly, TWO of the following terms: Data Flow architectures, Superscalar architectures, and Loosely-Coupled multiprocessor systems.

- a) A computer has a two-level virtual memory system. Its main memory M1 and secondary memory M2 have access times TA1 and TA2, of 0.1 msec and 5 msec respectively. It was found by measurement that the average access time for the memory hierarchy, TA, is 1 msec , which is considered unacceptably high. Describe the different approaches that could be used to reduce the access time from 1 msec to 0.5 msec , and discuss the hardware and software costs involved in **THIS** specific case.

- b) Describe **ONE** of the following structures: **Associative Memories** or **Interleaved Memories**

- a) Consider the following sequence of page address requests generated by a two-level virtual memory system using the Least Recently Used (LRU) replacement policy. (i.e. page 1 is requested, then page 2, ...)

1 2 3 1 3 4 1 5 2 1 6 1 3 1 7 4 1 2 8 1

Compute the hit ratio assuming that the main memory has a capacity of 4 pages.

- b) Describe TWO of the following interfaces: Extended Integrated Drive Electronics (EIDE), Small Computer System Interface (SCSI), Peripheral Component Interconnect (PCI), RS-232, or IEEE-488.

- a) List the main features of **ONE** of the following storage devices: Recordable CD ROM, DVD ROM, memory stick, or compact flash memories.

- b) Estimate the average latency and the total capacity of a moving-arm double-sided disk-storage device with 8 platters, 4096 tracks per surface, 63 sectors per track, 512 bytes per sector. The disk rotation speed is 7200 revolutions per minute.

- a) Consider a 32-bit adder constructed of four 8-bit carry-look-ahead adders connected via ripple-carry propagation. Compare the above adder to a standard 32-bit ripple-carry adder in terms of maximum delay.
- b) Draw a simple block diagram of a 4-bit hardware array multiplier. How are negative numbers handled?

- a) Consider the problem of replacing a non-pipelined ALU by a new 3-stage pipelined one. The new processing elements: PE0, PE1, and PE2 have execution times of $T/4$, $T/2$, and $T/4$ respectively, where T is the execution time of the original non-pipelined ALU. What is the speed-up factor with the new pipelined ALU? Suggest two ways to improve the performance further.
- b) What are the main differences between Reduce Instruction Set Computer (RISC) and Complex Instruction Set Computers (CISC)?

a) When is it more appropriate to use a microprogrammed control unit instead of a Hardwired one?

b) Compare the following design methods for hardwired control units: the **State-Table** method and the **Delay Elements** method.

c) Draw a simple block diagram of a **microprogrammed** control unit.

- a) Due to the **high level of pipelining** in modern computers, the execution of the branching instructions is unacceptably high. Describe the various approaches used by computer designers to overcome this problem?
- b) What are the advantages and disadvantages of using **assembly language programming** instead of a **high-level language** such as C++.
- c) What are the differences between a **compiler** and an **assembler**?

a) Why is Direct Memory Access (DMA) faster than **Programmed IO**?

b) What are the differences between **Vectored** and **Auto-Vectored Interrupts**?

c) What are the main differences between a **Software Interrupt** and a **Hardware Interrupt**?