National Exams, December 2002

98-Elec-B6, Integrated Circuit Engineering

3 hours duration

Notes:

If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made.

Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book exam.

Any five questions constitute a complete paper. Only the first five questions as they appear in your answer book will be marked.

All questions are of equal value. Marks for individual parts of questions are listed where appropriate.

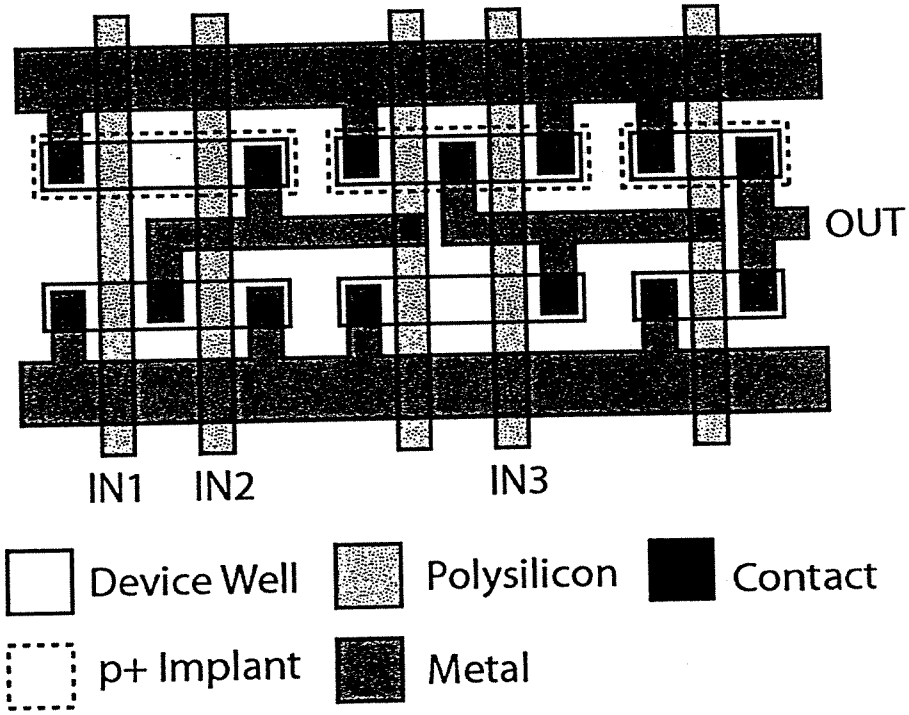
MOSFET drain current equations ($k = k_n$ for n-channel, k_p for p-channel)

$$I_D = \frac{W}{L} k \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad \text{triode}$$

$$= \frac{W}{L} k \frac{(V_{GS} - V_T)^2}{2} \quad \text{saturation}$$

Question 1. (Total 20 marks)

The layout of a CMOS integrated circuit is shown below, along with identification of layers. In order to make the diagram more readable, not all the layers required for a complete modern CMOS process are shown.



(a) (**10 marks**) Extract the transistor level schematic of this circuit.
(b) (**5 marks**) Determine the gate-level function of the circuit.
(c) (**5 marks**) Give two examples of masks not shown in the layout but which would be required for a modern CMOS process. Explain carefully what the masks are used for and why the steps are required.

Question 2. (Total 20 marks)

Discuss in detail (approximately one page) any four of the terms or topics given below. Your answer should concentrate on the context of an integrated circuit CAD environment. Each definition is worth 5 marks, and all are equally weighted.

(a) Logic synthesis.
(b) Mask-programmable arrays.
(c) Design rule checking.
(d) Floor planning.
(e) Timing simulation.
(f) Simulation vs. verification.
(g) Module generators.

Question 3. (Total 20 marks)

In modern MOS devices, a number of second order effects must be considered for accurate prediction of circuit behavior. For any four of the effects below, discuss the physical origin of the effect and its influence on MOS transistor behavior.

(a) Threshold variation
(b) Source-drain resistance
(c) Velocity saturation
(d) Mobility degradation
(e) Subthreshold conduction

Question 4. (20 Marks)

Starting from a bare silicon surface, show the processing steps which would be required to fabricate a pair of complementary devices in an n-substrate, p-well CMOS technology. Assume the p-well has already been fabricated. Clearly depict the role of masks in the process flow. A complete fabricated structure will include n- and p-channel transistors as well as contact cuts and metal connections to the source and drain regions of each device. Substrate or split contacts are not required. Use a series of cross-sections showing development of the required structures and layers to show the process flow.

Question 5. (Total 20 marks)

(a) **(14 marks)** Show that the propagation delay of a simple CMOS inverter driving a capacitive load C_L can be approximated by the expression shown below. (*Hint*: assume each device is in saturation during the relevant transient).

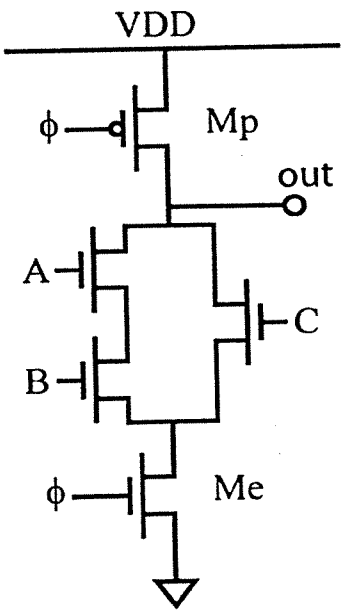
$$t_p \approx \frac{C_L}{2V_{DD}}\left(\frac{1}{k_p}+\frac{1}{k_n}\right)$$

(b) **(3 marks)** Why does increasing the width to length ratios of the transistors decrease the propagation time?

(c) **(3 marks)** Is there any limit to this effect, i.e., can the propagation time be reduced to an arbitrarily small value simply by scaling the transistors? If not, why not?

Question 6. (20 Marks)

The schematic diagram of a dynamic CMOS gate is shown below.



(a) **(11 marks)** Explain the operation of this gate during precharge and evaluation phases. What is the logic function provided by this gate?
(b) **(5 marks)** Give two advantages of dynamic CMOS logic over static logic.
(c) **(4 marks)** Describe either the charge leakage or charge sharing problem in dynamic CMOS logic gates.

Question 7. (20 Marks)

(a) **(8 marks)** As the power supply of a CMOS gate or macrocell is decreased, both the normalized power-delay product and normalized delay are affected. Sketch typical characteristics for these quantities with respect to power supply.
(b) **(6 marks)** Does lowering the threshold voltages of the transistors increase or decrease the delay at a given power supply value, and why?
(c) **(6 marks)** How can the effective capacitance be lowered in a practical circuit to reduce delay? Your answer should address both physical capacitance and switching activity.