

**National Exams – May 2003**

**98-Elec-A4, Digital Systems and Computers**

**3 Hours Duration**

**NOTES**

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made;
2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a Closed Book exam.
3. Any five questions constitute a complete paper. Only the first five questions as they appear in your answer book will be marked.
4. All questions are of equal value

1. Considering the Karnaugh map shown below for variables A, B, C, and D.
- Draw the Truth Table, which the K map represents.
  - Write the min term expression  $f(A, B, C, D) = \sum m ( \quad )$ .
  - Write the minimum logical function derived from the K-map, and
  - Draw the logic gate architecture, which realizes the logical function obtained in c).

	AB			
CD	00	01	11	10
00	1	0	1	0
01	1	1	0	1
11	1	0	1	1
10	0	1	0	0

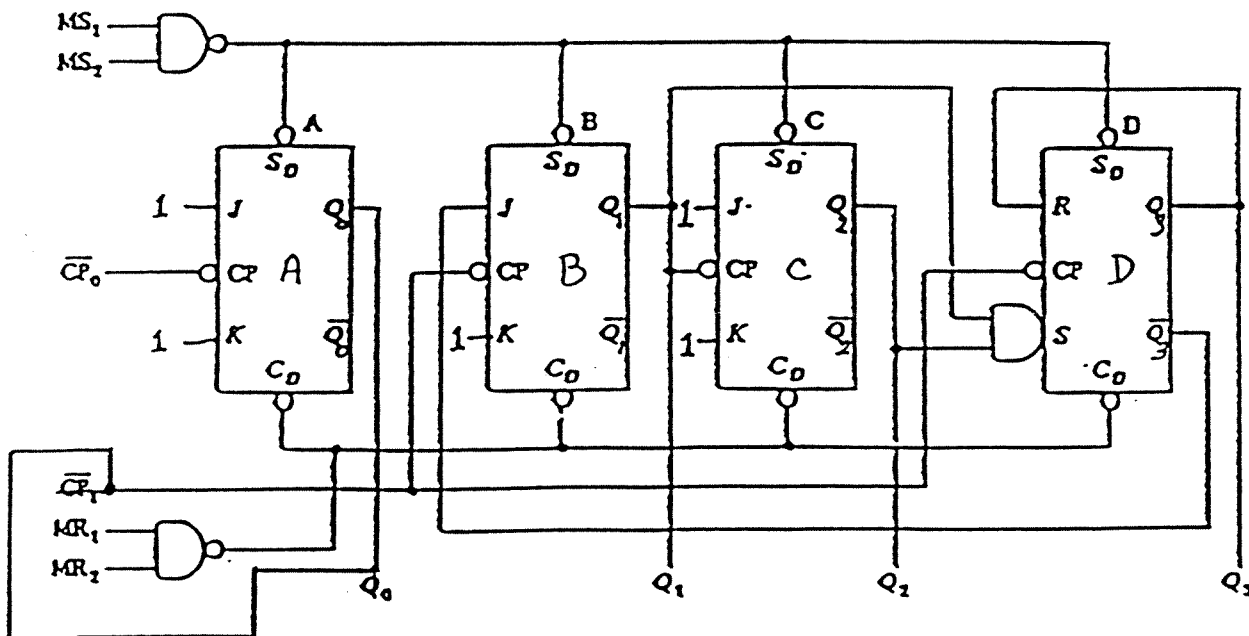
2. The following circuit represents a 7490-decade counter. The inputs are explained as follows:

- MS<sub>1</sub>, MS<sub>2</sub>: Master Set Controls (i.e.: Preset)
- MR<sub>1</sub>, MR<sub>2</sub>: Master Reset Controls (i.e.: Clear)
- $\overline{CP_0}$ : Clock (active low) for FFA alone
- S<sub>D</sub>: Direct set
- C<sub>D</sub>: Direct clear
- $\overline{CP_1}$ : Clock (active low) for FFB and FFD

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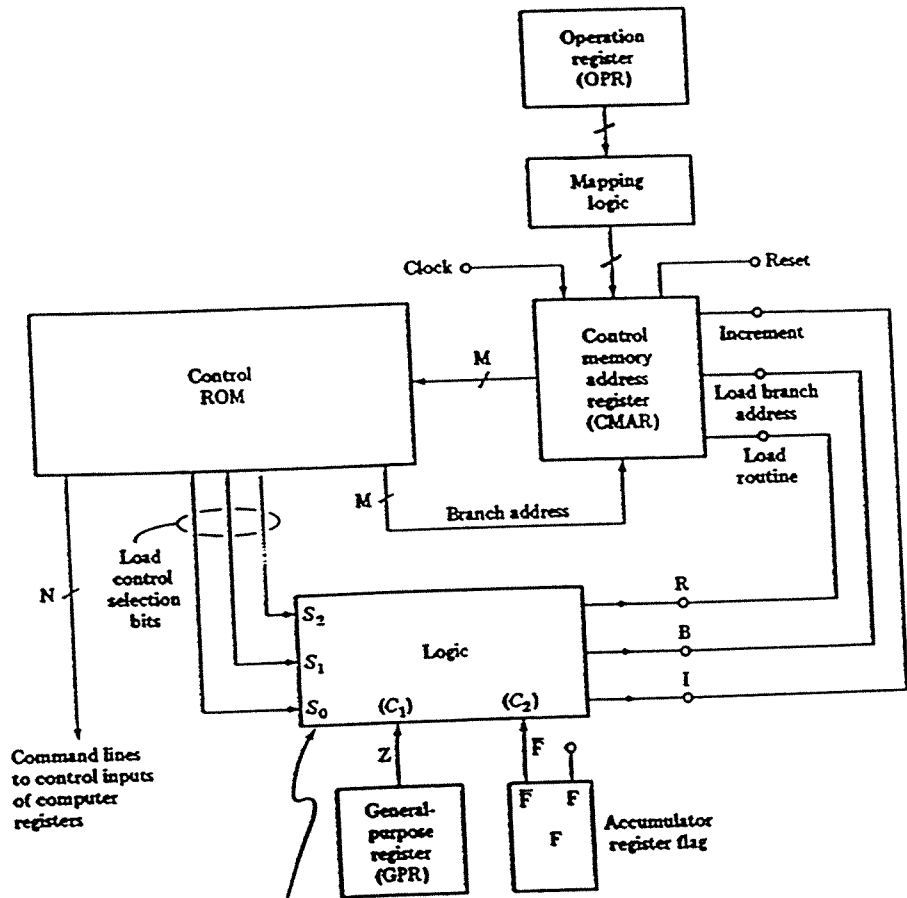
Using 12 clock cycles, construct the timing diagram showing the state of the Q's of the four flip-flops during the twelve clock cycles. Assume that MS<sub>1</sub>, MS<sub>2</sub>, MR<sub>1</sub>, and MR<sub>2</sub> are at levels which allow the counter to operate in a synchronous mode. Also, note that Q<sub>0</sub> is connected externally to  $\overline{CP_1}$ .

The train of pulses to be counted is applied to  $\overline{CP_0}$  and all FFs trigger on the negative or trailing edge of the pulse applied at their clock input. Assume that the propagation delays through all combinational gates and flip-flops are zero.



3. The following architecture represents a ROM controller for a microcomputer. The logic box in the controller with inputs  $S_2, S_1,$  and  $S_0$  (load control section bits) and  $C_1, C_2$  (status bits), has to be designed using combinational logic gates. Considering that the truth table for this logic box is given at the bottom of the circuit, draw the minimum circuit necessary to implement the truth table.

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$S_2$	$S_1$	$S_0$	$C_1$	$C_2$	B	I	R
0	0	0	x	x	0	1	0
0	0	1	x	x	1	0	0
0	1	0	0	x	1	0	0
0	1	0	1	x	0	1	0
0	1	1	x	0	0	1	0
0	1	1	x	1	1	0	0
1	x	x	x	x	0	0	1

4. The Transition Table of a controller to be designed is as follows:

Present State	Present State			Next State	
	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	X = 0	X = 1
0	0	0	0	000	001
1	0	0	1	010	001
2	0	1	0	011	011
3	0	1	1	100	100
4	1	0	0	101	101
5	1	0	1	110	110
6	1	1	0	000	000

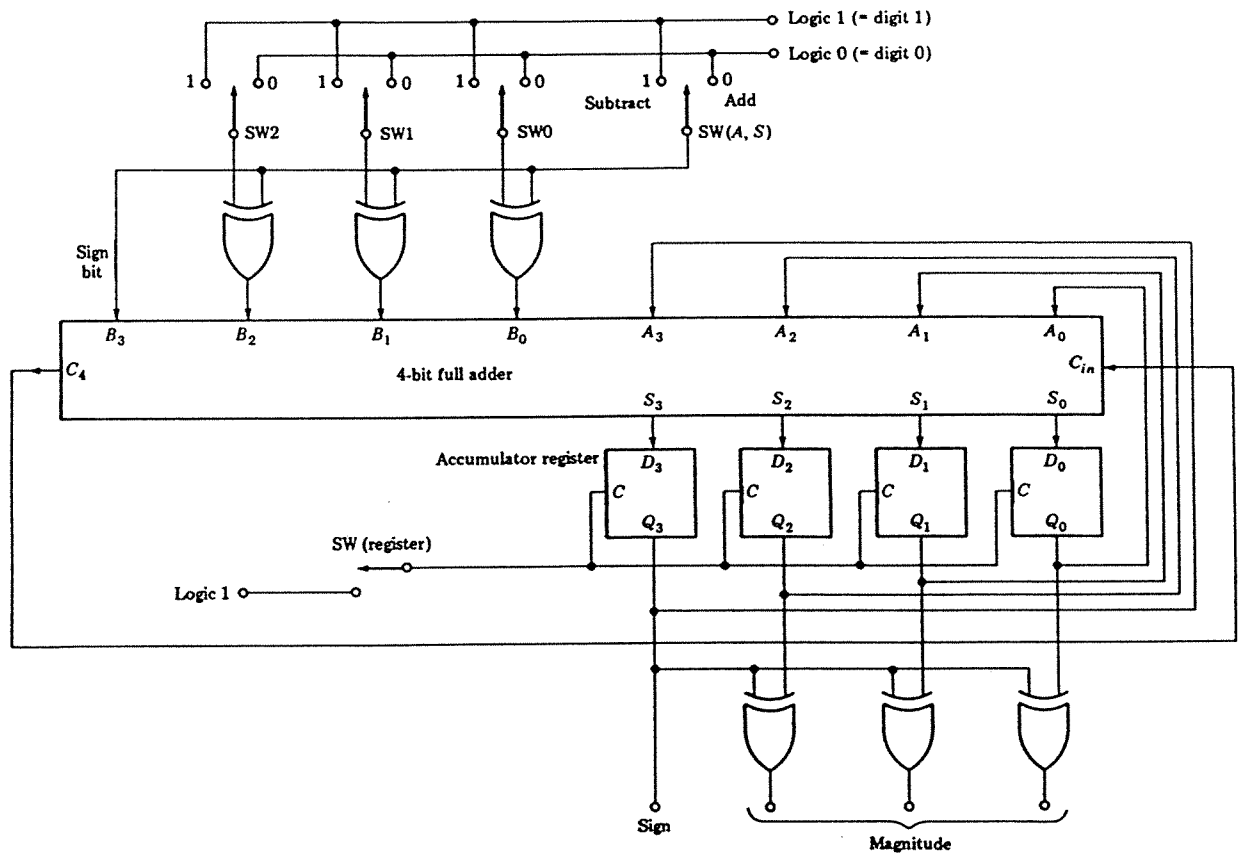
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- Draw the K maps representing the inputs to the number of D flip-flops necessary to execute this transition table. X is an input to the controller from an external source.
- From the K maps you have drawn, write the logical function representing each of the required D inputs.

5. The following digital circuit represents an adder/subtractor which has the capability of operating on decimal numbers covering the range of  $\pm 7$ . Explain how the circuit can perform the following arithmetical operations by explaining the use of ones-complement.

- a) -6-1 (i.e.: minus six added to minus one)
- b) 4-5 (i.e.: plus four minus five).
- c) How could the circuit be modified to add two eight bit numbers as large as 200 and 100 together?

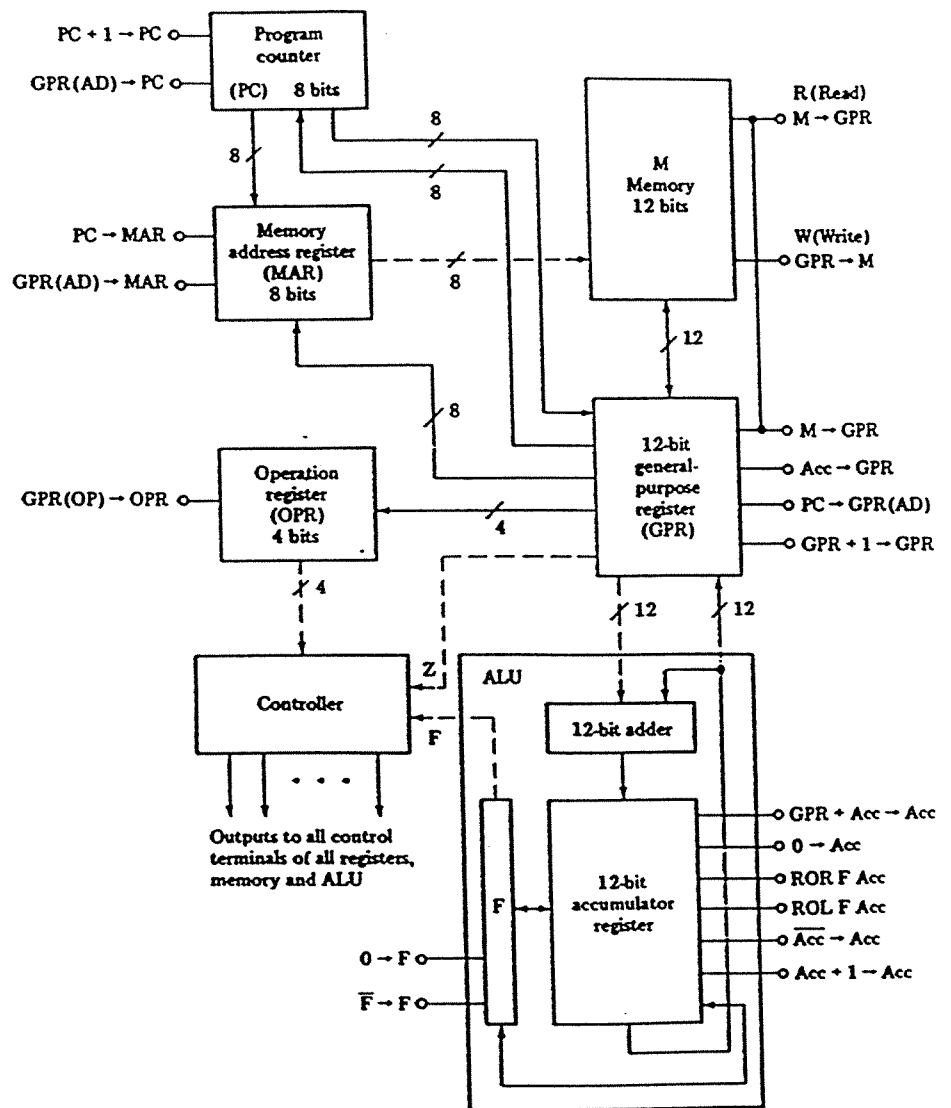
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6. Considering that the architecture of a microcomputer is as shown below, write the microoperations necessary to carry out the following instructions. Assume that the fetch part of the cycle has been completed.

- a) JMP – Jump
- b) JMPI – indirect jump
- c) CSR – call
- d) ISZ – Increment and skip if zero

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Note: In answering this question, explain first what each instruction is intended to do, and also indicate how much time it takes to execute each instruction assuming that the clock rate is 1.25MHz.