

National Exams May 2003

98-Elec-A5, Electronics

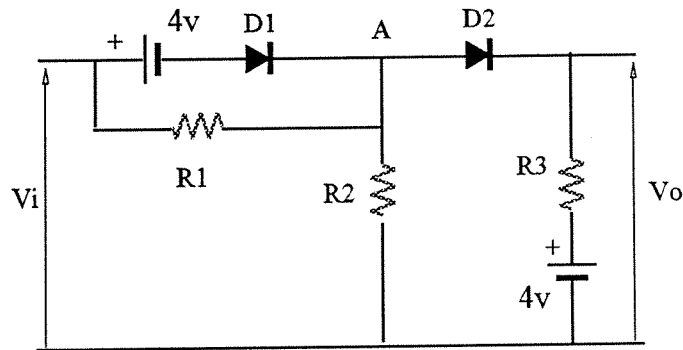
3 hours Duration, Closed Book

Notes:

1. If any doubt exists as to the interpretation of any question, the candidate is urged to submit, within their answer, a clear statement of any assumptions made.
2. This is a "Closed Book" Examination.
3. Candidates may use one of two calculators, the Casio or Sharp approved models.
4. Any 5 (FIVE) questions constitute a complete paper. Only the first five questions presented for evaluation will be marked.
5. All questions are worth 20 marks each.
6. When asked to "Derive an Expression", no marks will be credited for any formula stated without any proof.
7. Please start each question on a new page and clearly identify the question number and part number, e.g. Q4(a).
8. In schematics, ground and chassis may be assumed to be common, unless specifically stated otherwise.
9. Unless otherwise specified, assume that Op-Amp supply voltages are $\pm 15V$.
10. A sheet of semi-log graph paper is attached as last page.

1. [20 Marks]

In the diode circuit shown below, $R_1 = R_3 = 10\text{ K}\Omega$, $R_2 = 20\text{ K}\Omega$ and the diodes may be considered to be ideal.



- (a) Plot the v_o/v_i transfer characteristic for the circuit for $-20\text{v} \leq v_i \leq +20\text{v}$.
Clearly annotate the graph showing all breakpoints and all significant values. [16 Marks]
- (b) Sketch the output waveform that results when a voltage, which repeatedly ramps linearly between $-20\text{v} \leq v_i \leq +20\text{v}$, is applied as input. [4 Marks]

Clearly state and justify all assumptions made

2. [20 Marks]

- (a) Sketch a circuit using a Zener Diode to provide a simple regulated voltage supply and explain the purpose of every component in your circuit. [5 Marks]
- (b) A particular integrated circuit, for which $60\text{mA} \leq I_L \leq 75\text{mA}$, requires that its supply voltage be in the range $3.0\text{v} \leq V_L \leq 3.6\text{v}$. Show how this may be achieved using a battery comprising three 1.5v rechargeable cells and a Zener diode with $V_{\text{knee}} = 3.1\text{ volt}$ and $R_Z = 25\ \Omega$. [12 Marks]
- (c) What prevents the Zener diode from being damaged if the device is accidentally disconnected? [5 Marks]

3. [20 Marks]

A J-FET having $I_{DSS} = 12\text{mA}$ and $V_P = -4\text{V}$ is to be used in a common-source amplifier with a [mid-band, ac voltage gain] ≥ 4 when connected between a source with output resistance of $100\text{k}\Omega$ and a $10\text{k}\Omega$ load resistance.

Assume that $r_d = 40\text{k}\Omega$ and that :

$$I_{DS} = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 \quad \text{for } |V_{GS}| \leq |V_P|$$

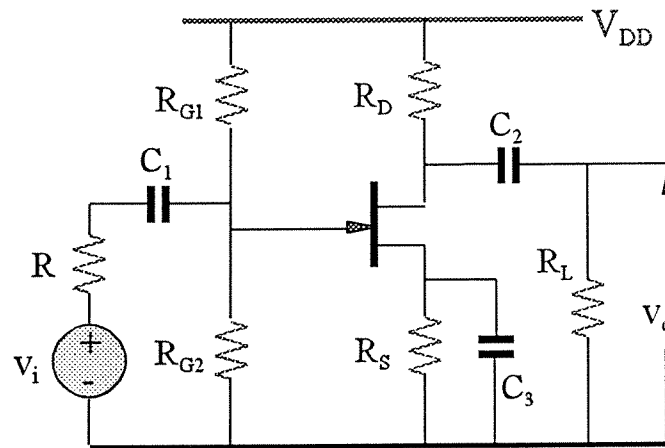
- (a) Sketch a circuit diagram, using preferred biasing, for this amplifier and provide values for all the resistors used with a 15volt power supply. [6 Marks]
- (b) Determine the quiescent values of all node voltages and all branch currents in your circuit. [10 Marks]
- (c) Calculate the actual value of the overall voltage gain of your amplifier. [6 Marks]

Justify all values.

4. [20 Marks]

For the circuit shown below:

1. Derive an expression for the overall voltage gain to show the effect of C_1 if it is assumed that C_2 and C_3 have very large values. [6 Marks]
2. Derive an expression for the overall voltage gain to show the effect of C_2 if it is assumed that C_1 and C_3 have very large values. [8 Marks]
3. Calculate suitable values for C_1 and C_2 so that the overall voltage gain of the amplifier does not drop more than 3dB below its mid-band values for any frequency above 50Hz. Assume C_3 is very large. [6 Marks]



$R = 10\text{K}\Omega$	$R_{G1} = 480\text{K}\Omega$	$R_{G2} = 120\text{K}\Omega$
$R_D = 3\text{K}\Omega$	$R_S = 2\text{K}\Omega$	$R_L = 10\text{K}\Omega$
$I_{DSS} = 12\text{ma}$	$V_P = -4\text{v}$	$r_D = 40\text{K}\Omega$

5. [20 Marks]

(a). For the circuit shown below, assume that C_1 and C_2 are very large and derive symbolic expressions for the mid-band values of:

(i) the input resistance, and [6 Marks]

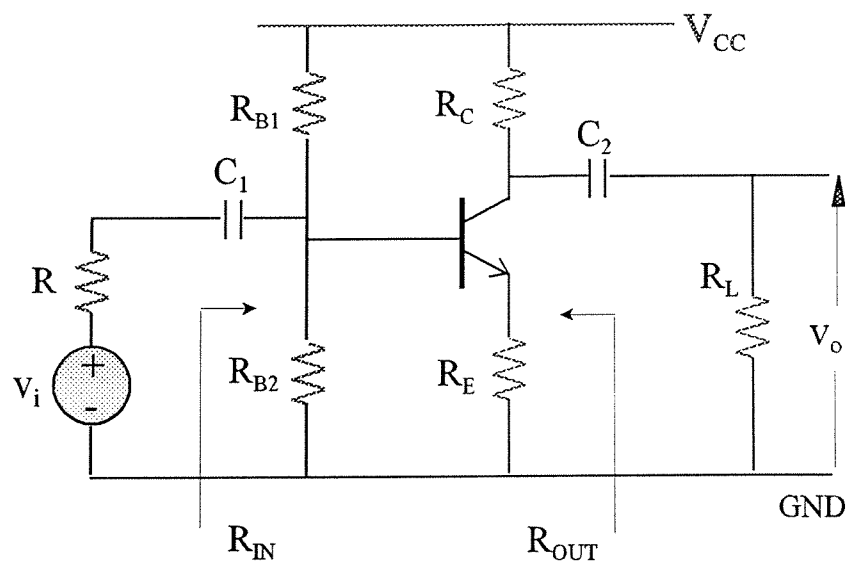
(ii) the output resistance. [10 Marks]

A proof must be provided for any formula used.

(b) Evaluate both these expressions. [4 Marks]

Assume that the transistor has significant parameters: $\beta = 50$ and $r_{\pi} = 1500\Omega$.

All other assumptions must be clearly stated and justified.



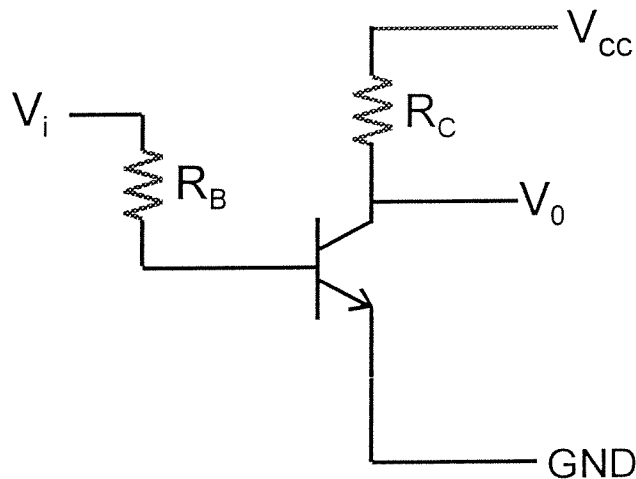
Other component values are :

$$R_{B1} = 72\text{K}\Omega, \quad R_{B2} = 18\text{K}\Omega, \quad R_C = 4\text{K}\Omega, \quad R_E = 1.4\text{K}\Omega,$$

$$V_{CC} = 15\text{v}, \quad R = 1\text{K}\Omega, \quad \text{and} \quad R_L = 10\text{K}\Omega.$$

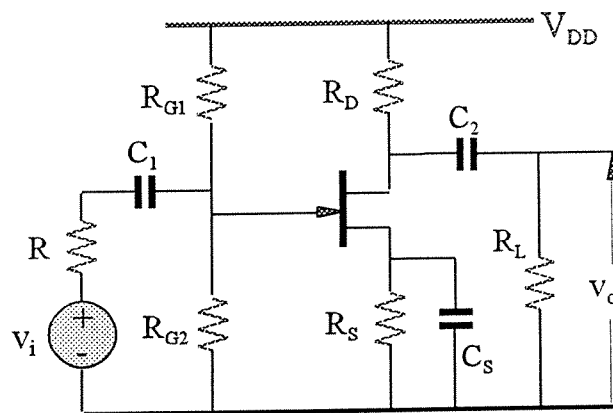
6. [20 Marks]

- (a) Define the terms: (i) Overdrive factor, (ii) Fan out and (iii) Noise Margins. [6 Marks]
- (b) A logic inverter, intended for use in a noisy environment, and to be operated from a 12 volt supply is shown below. Determine a suitable value for R_B such that the inverter has an overdrive factor of 4 and a fan out of 8 when using $R_C = 5\text{K}\Omega$ with a transistor for which $\beta = 50$ and $V_{BE} = 0.7$ volt and $V_{CE(\text{sat})} = 0.2$ volt. [6 Marks]
- (c) Calculate the value of V_o when V_i is LOW and the inverter is driving 8 loads. [4 Marks]
- (d) Using the value of R_B calculated in (b), determine the new values of fan out and overdrive if the transistor is replaced by another having: [4 Marks]
- (a) $\beta = 25$ and (b) $\beta = 100$.




7. [20 Marks] For the FET amplifier shown below :
- Determine the quiescent values of I_D , I_{RL} , V_D , V_G , V_S , and V_{GS} . [6 Marks]
 - Derive an expression, that includes R_S and C_S , for the overall voltage gain (v_o/v_i). Prove any formulae used. [6 Marks]
 - Determine the maximum amplitude of the sinusoidal input signal that can be applied without causing distortion at the output when C_S is removed. [3 Marks]
 - Calculate the value of C_S such that the voltage gain, for all frequencies above 30 Hz, will be no more than 3dB below the value of the gain at mid-band. [Neglect all high frequency effects.] [3 Marks]
 - Plot the gain-frequency response at low and mid frequencies. [An annotated Bode plot is acceptable, and high frequency effects are neglected] [2 Marks]

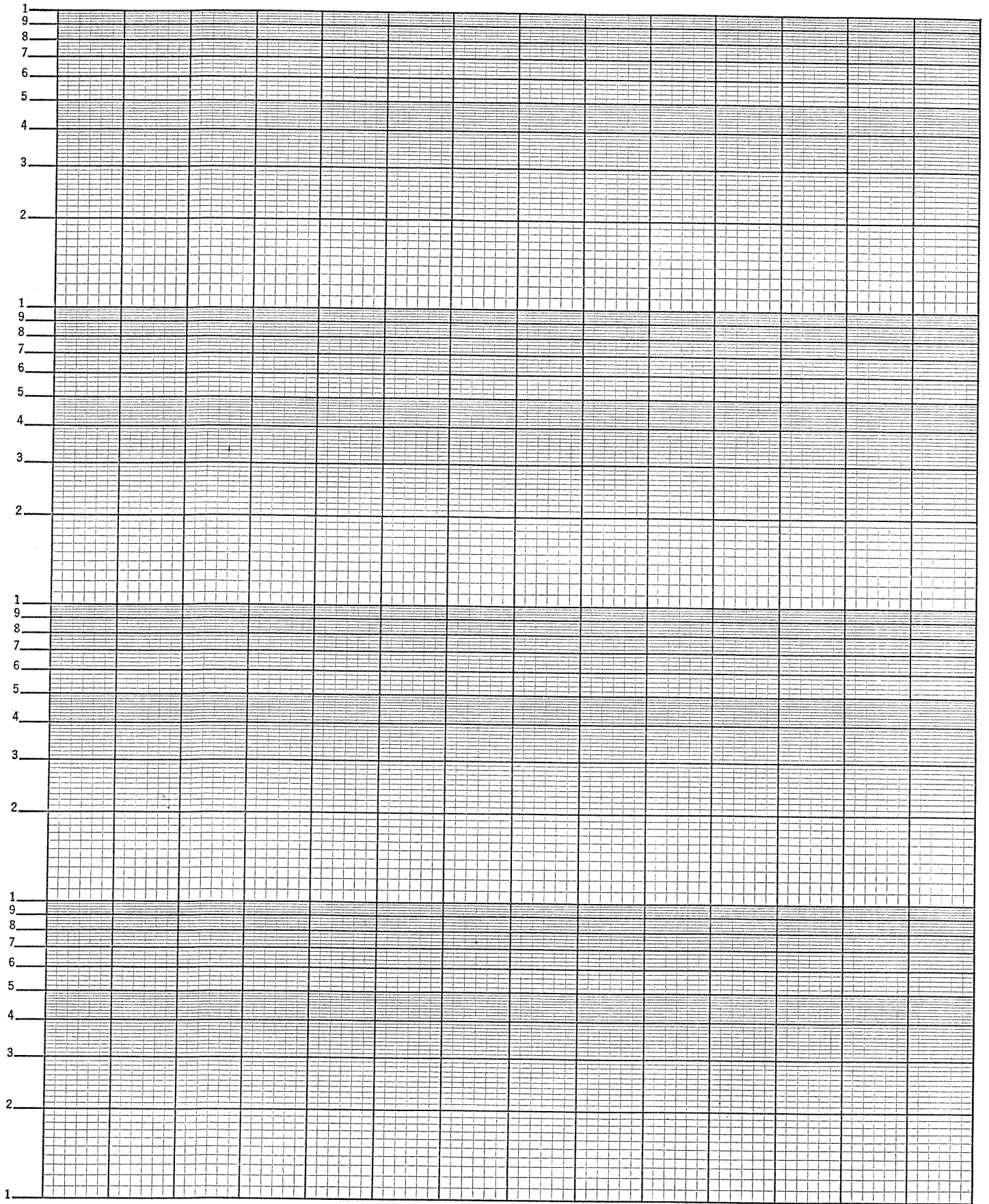
Assume: $R = 100K\Omega$ $R_{G1} = 1M\Omega$ $R_{G2} = 180K\Omega$
 $R_D = 10K\Omega$ $R_L = 10K\Omega$ $V_{DD} = +25v$
 $g_m = 2mA/V$ $I_{DSS} = 16A$ $V_P = -4v$ $r_d = 40K\Omega$
 $C_1 = \text{Large}$ $C_2 = \text{Large}$ $C_S = ?$



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4 CYCLES X 8 1/2 DIVISIONS
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