

National Exams December 2003

98-BS-8, Digital Logic Circuits

3 hours duration

NOTES:

1. If a doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made with the answer of the question.
2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a closed book examination, however, candidates are allowed to bring the following into the examination room.
 - (i) One hand-written information sheet (8.5" X 11") of self prepared notes.
3. Any **FOUR (4)** questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.
4. All questions are of equal marks. Total marks = 100
5. This paper contains **Six (6)** questions and comprises **Eight (8)** pages.
6. Each question carries 25 marks and marks for each question part are indicated in brackets.
7. Data on some relevant Digital ICs are provided in the Appendix.

1. (a) Determine the Boolean expression for output Z of the circuit given in Figure Q1. Simplify the expression using Boolean algebra.

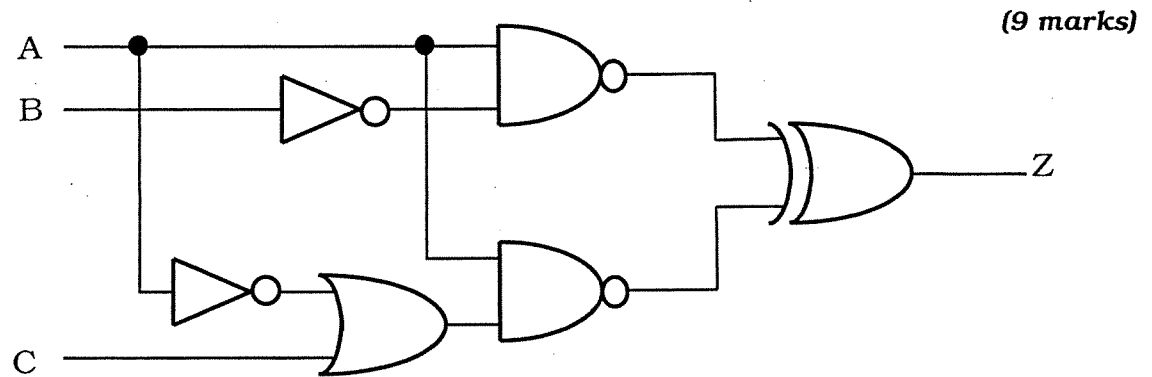


Figure Q1

- (b) Simplify the switching function, F by using K-map method.

$$F(A, B, C, D) = \prod M(1, 3, 4, 5, 6, 7, 9, 10, 11, 15)$$

(16 marks)

- (i) Draw the K-map for the function, F.
 (ii) Simplify the switching function, F and write a simplified Boolean expression in POS form.

2. A small corporation has 14 shares of stock, and each share entitles its owner to one vote at stockholder's meeting. Three people own the 14 shares of stock as follows:

| | |
|--------|----------|
| Mr. A: | 6 shares |
| Mr. B: | 3 shares |
| Ms. C: | 5 shares |

Each stockholder has to close a switch when voting *yes* and to open it when voting *no* for his/her shares as shown in Figure Q2. The outputs of the voting logic circuit present the total number of shares that vote *yes* for each measure.

- (a) Represent the voting logic circuit problem in terms of a truth table. (5 marks)
- (b) Develop and simplify the Boolean expressions for all the outputs of voting logic circuit. (12 marks)
- (c) Implement the voting logic circuit by using a PAL16L8 given in the appendix. (8 marks)

Figure Q2 on Page 3

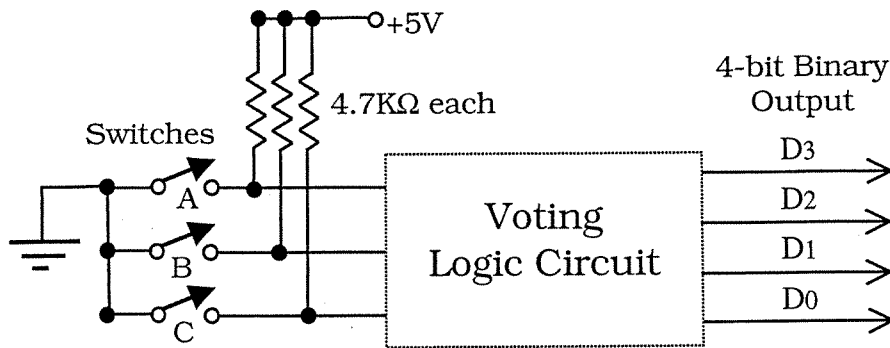


Figure Q2

3. Provide a brief answer for the following questions with justification.

a) If a digital system has 5 inputs, how many possible input combinations are there?

(3 marks)

b) Which of the following binary values is closest to the decimal value $(1.01)_{10}$.

- i. $(1.01)_2$
- ii. $(1.0001)_2$
- iii. $(1.001010001)_2$
- iv. $(1.0000001)_2$

(4 marks)

c) If $A = 1$, $B = 0$, and $C = 1$, then find X where $X = \overline{(A \oplus B)} + C$

(5 marks)

d) Identify the clocked flip-flop described in the following characterization table.

| Inputs | | Output |
|--------|---|-----------------|
| A | B | Q_{n+1} |
| 0 | 0 | Q_n |
| 1 | 0 | 0 |
| 0 | 1 | $\frac{1}{Q_n}$ |
| 1 | 1 | Q_n |

(6 marks)

e) Determine the clocked flip-flop described in the following excitation table. X in the table represents don't care conditions.

| Q_n | Q_{n+1} | Inputs | |
|-------|-----------|--------|---|
| | | A | B |
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | X | 0 |

(7 marks)

4. (a) Study the JK flip-flop circuit of Figure Q4 given below.

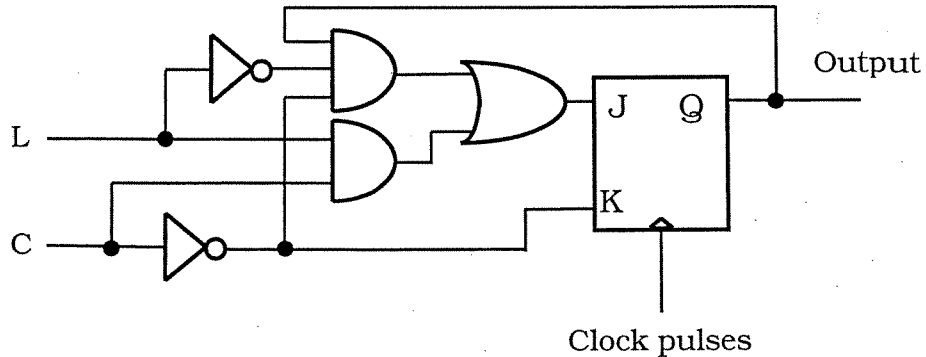


Figure Q4

Determine the output, Q at positive clock transitions for all the combinations of inputs, L and C .

(9 marks)

- (b) Suppose the three joints (shoulder, elbow and wrist) of a robot arm are to be flexed in a sequence, i.e. shoulder first, followed by elbow and then wrist. The robot control has three TTL inputs S , E and W and high-level TTL signals on these inputs flex their particular joints.

Using a suitable size binary counter, decoder and/or additional gates, implement a digital circuit that flexes the robot joints repeatedly in a sequence given below:

- Shoulder for 30 ms
- Elbow for 10 ms
- Wrist for 20 ms

Ignore any decoding glitches and assume that a 100Hz TTL clock signal is available.

(16 marks)

5. (a) Design a 3-bit synchronous counter that has the following sequence: 000, 010, 101, 110, 100, and repeat. The unused states 001, 011, and 111 must always go to 000 state on the NEXT clock pulse. Use positive edge triggered D-type flip-flops.

(10 marks)

Question No. 5 continues on Page 5

- (b) Redesign the counter of part (a) without any requirement on the unused states; that is, their NEXT states can be don't cares. Compare this redesigned counter with the design of part (a). **(15 marks)**

6. (a) Develop a sequential circuit that delays a serial TTL data signal by $14\mu\text{sec}$. Implement an economical sequential (delay) circuit by using suitable gates, flip-flops, shift registers and/or counters. The block diagram of the circuit along with its input/output signals is shown in Figure Q6. Assume that a 2MHz TTL clock is also available. **(18 marks)**

- (b) Justify that the delay circuit designed in part (a) uses minimum amount of hardware. Identify at least two useful applications of the delay circuit. **(7 marks)**

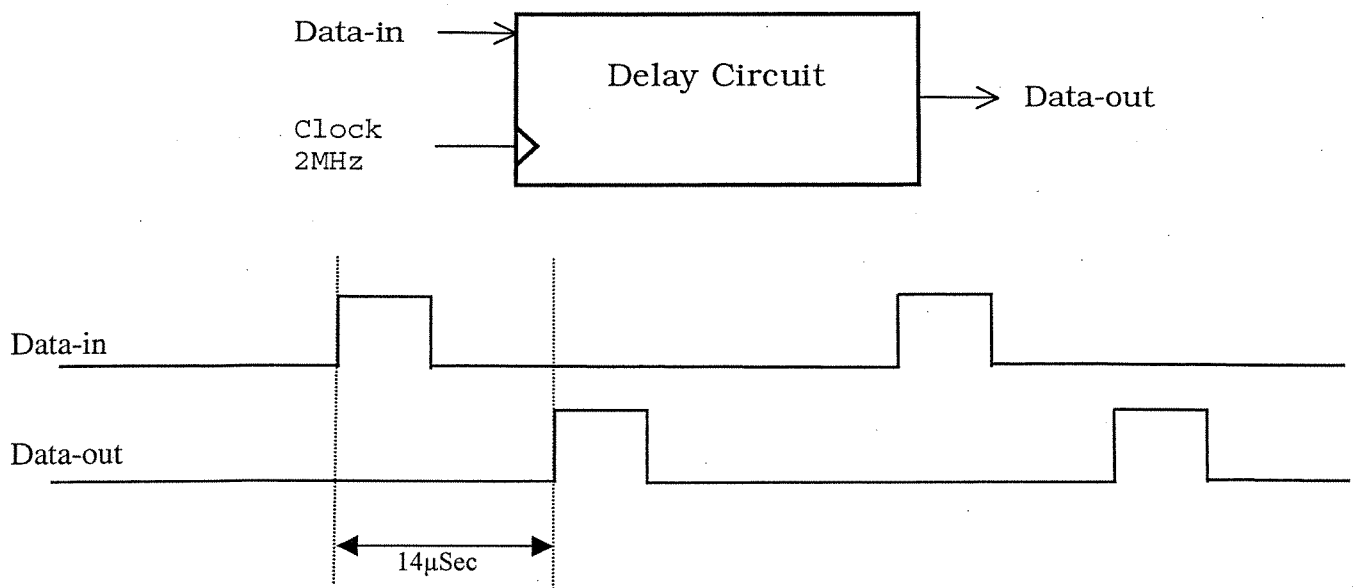
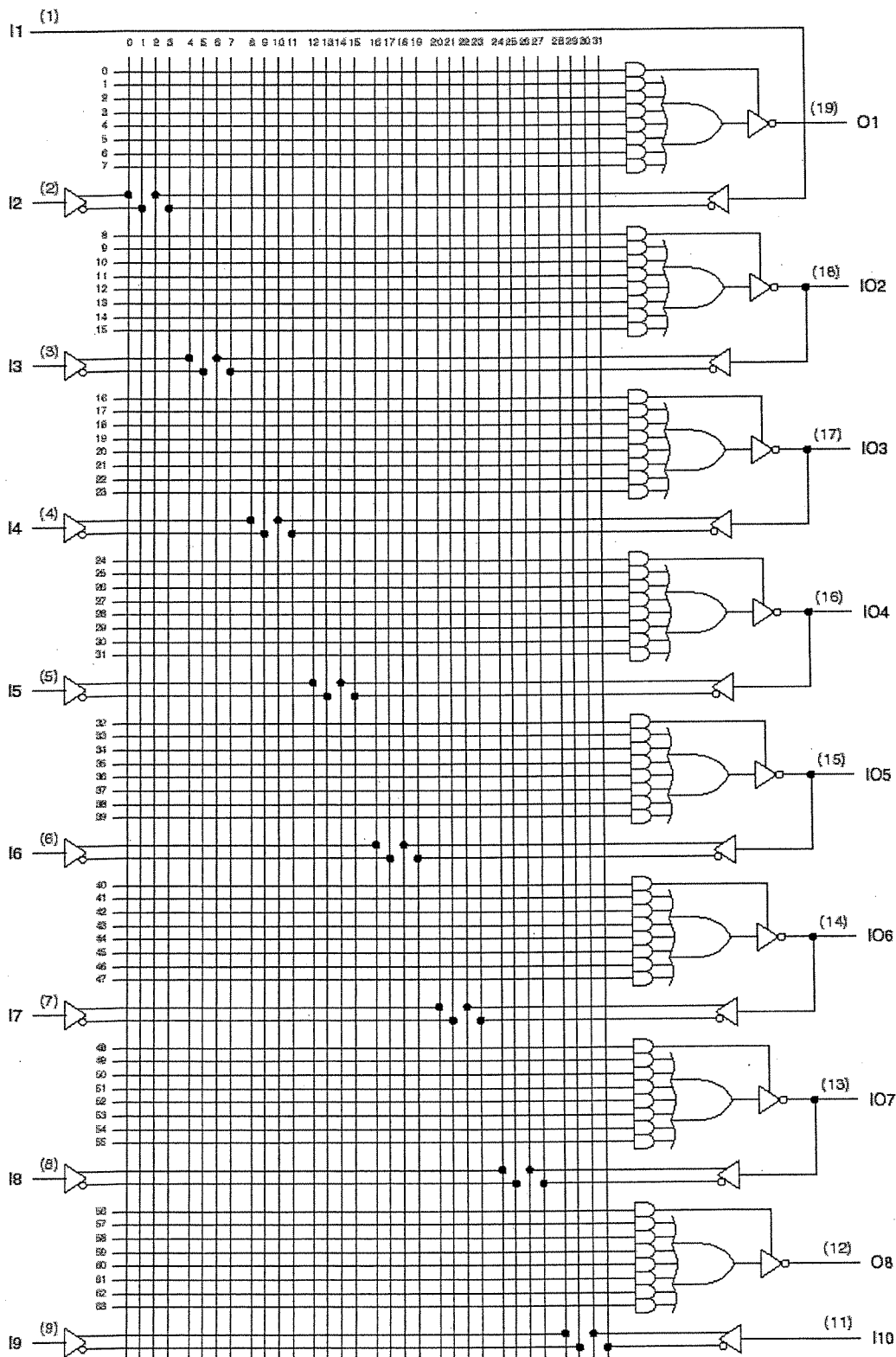


Figure Q6

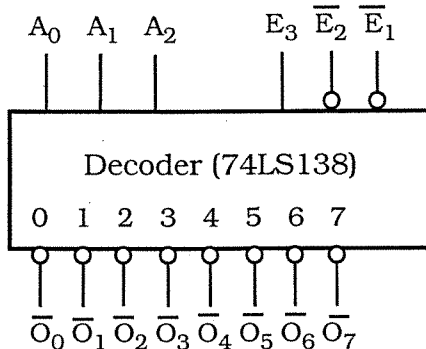
APPENDIX

PAL16L8



Decoder, Counter, MUX and Shift Register Data Sheets

74LS138: 3-to-8 Decoder



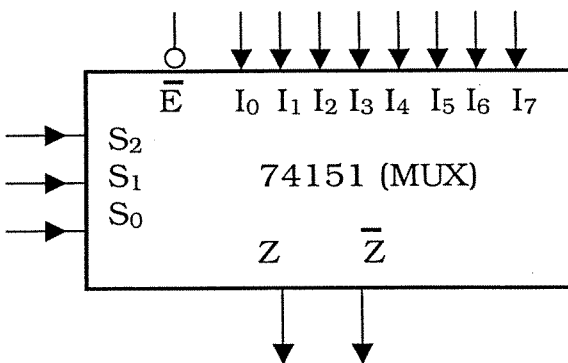
| Inputs | | | Outputs |
|------------------|------------------|-------|-----------------------------------|
| \overline{E}_1 | \overline{E}_2 | E_3 | |
| 0 | 0 | 1 | Respond to input code $A_2A_1A_0$ |
| 1 | x | x | Disabled - all HIGH |
| x | 1 | x | Disabled - all HIGH |
| x | x | 0 | Disabled - all HIGH |

74151: 8-to-1 Multiplexer

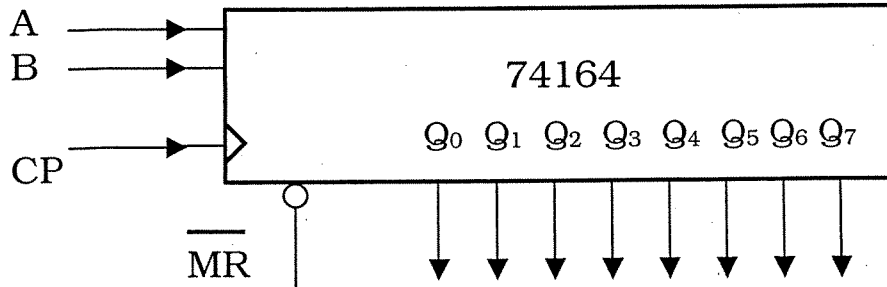
Inputs

Outputs

| \overline{E} | S_2 | S_1 | S_0 | Z | \overline{Z} |
|----------------|-------|-------|-------|------------------|----------------|
| H | X | X | X | H | L |
| L | L | L | L | \overline{I}_0 | I_0 |
| L | L | L | H | \overline{I}_1 | I_1 |
| L | L | H | L | \overline{I}_2 | I_2 |
| L | L | H | H | \overline{I}_3 | I_3 |
| L | H | L | L | \overline{I}_4 | I_4 |
| L | H | L | H | \overline{I}_5 | I_5 |
| L | H | H | L | \overline{I}_6 | I_6 |
| L | H | H | H | \overline{I}_7 | I_7 |

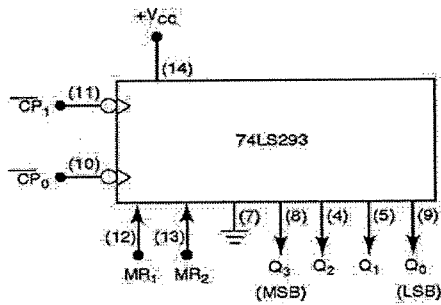
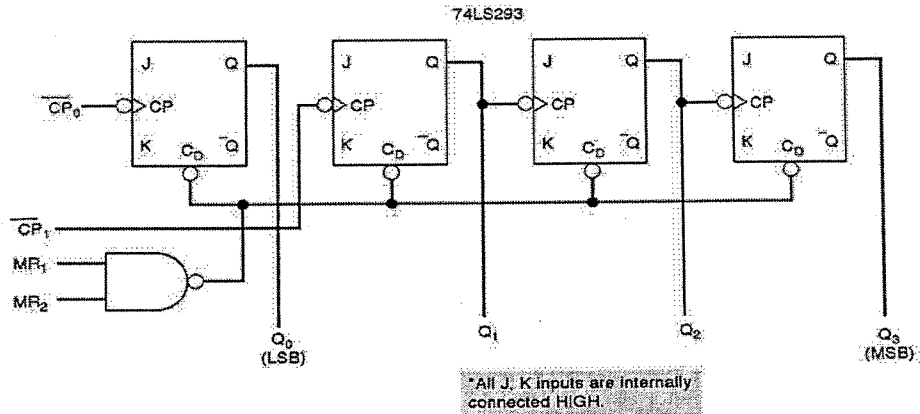


74164: 8-bit Shift Register



- An eight-bit shift register with all FF outputs $Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6$ and Q_7 are externally available.
- Inputs A and B are ANDED together to produce the serial input to flip-flop Q_0 .
- Shift operation occurs at PGTs of the clock input CP.
- The \overline{MR} input resets all FFs asynchronously on a LOW level.

74293 : 3/4-bit counter



End of Paper

PAL16L8

