

**PROFESIONAL ENGINEERS OF ONTARIO  
NATIONAL EXAMS DECEMBER 2003  
98-COMP-A3 (COMPUTER ARCHITECTURE)  
3 hours duration**

**NOTES:**

1. If doubt exists as to the interpretation of any question, the candidate is advised to submit with the answer paper a clear statement of any assumptions made;
2. Candidates may use one of the two calculators: the Casio or Sharp approved models. This is a Closed-Book exam
3. You must answer Q1 and any five (5) of the remaining questions.

NAME (Please print): \_\_\_\_\_

SIGNATURE: \_\_\_\_\_

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Question [1] 15 marks \_\_\_\_\_

Question [2] 17 marks \_\_\_\_\_

Question [3] 17 marks \_\_\_\_\_

Question [4] 17 marks \_\_\_\_\_

Question [5] 17 marks \_\_\_\_\_

Question [6] 17 marks \_\_\_\_\_

Question [7] 17 marks \_\_\_\_\_

TOTAL (out of 100) \_\_\_\_\_

**Q1- Architecture and programming [15 marks]**

- a) Describe three key concepts of the von Neumann architecture
- b) Give five major milestones in the evolution of the modern digital computer architecture. Explain each briefly.
- c) What is the difference between interpretation and translation? Explain.
- d) What is the difference between assembly language and machine language? Explain.
- e) What are some typical distinguishing characteristics of Reduced Instruction Set Computer (RISC) organization?

**Q2- CPU and Memory organization; buses [17 marks]**

- a) What are the advantages of using a memory cache? Under what circumstances (that is, for what program behaviors) would a cache be of no help?
- b) Assume that access to a cache on the processor takes 1 time unit. This access time is constant whether the item exists in the cache (i.e. cache hit) or not (i.e. cache miss). Further, assume that the access to the main memory takes 10 time units. Derive a formula for the average access time, depending on the cache hit rate  $p$ . Calculate the average access times for  $p=0$ ,  $p=0.9$  and  $p=0.99$ . At what minimum value for  $p$  will the average access time be less than in a system without a cache?
- c) A computer has a bus with a 25 nsec cycle time, during which it can read or write a 32-bit word from memory. The computer has a disk that uses the bus and runs at 40 Mbytes/sec. The CPU normally fetches and executes one 32-bit instruction every 25 nsec. How much does the disk slow down the CPU?

**Q3- I/O and interrupts [17 marks]**

- a) Why does a computer system need interrupts? List the three most common classes of interrupts. How are the multiple interrupts handled in a computer system?
- b) What are the advantages and disadvantages of programmed I/O versus DMA (Direct Memory Access)?
- c) In virtually all computer systems that include DMA modules, DMA access to main memory is given higher priority than CPU access to main memory. Why? Explain.
- d) When a device interrupt occurs, how does the processor determine which device issued the interrupt?

**Q4- Instruction sets and addressing modes [17 marks]**

- a) Describe where the operand of a given instruction is found and, where applicable, how its effective (physical) address is calculated in the following addressing modes:
  - i) Register
  - ii) Immediate
  - iii) PC-relative
  - iv) Displacement
- c) What are the typical elements of a machine instruction? What types of operands are typical in machine instruction sets? If an instruction contains four addresses, what might be the purpose of each address?
- d) Design a variable-length opcode to allow all of the following to be encoded in a 36-bit instruction:
  - Instructions with two 15-bit addresses and one 3-bit register number
  - Instructions with one 15-bit addresses and one 3-bit register number
  - Instructions with no addresses or registers

**Q5- Controller design, hardwired and microprogram control [17 marks]**

- a) When is it appropriate to use a microprogrammed control unit instead of a hardwired one?
- b) Explain the difference between horizontal and vertical microinstruction formats, and discuss the three major factors influencing the design of microinstruction's word length
- c) Compare the following design methods for hardwired control units: state-table method and delay elements method.
- d) List some common applications of microprogramming

**Q6- Assembly [17 marks]**

- a) Why would someone ever program in assembly language? List your reasons and explain them.
- b) Assume an assembler language with the following three statements:
  - `ADD R1, R2, R3`                   :R1=R2+R3  
(R1 contains the result of adding the contents of R2 and R3)
  - `SUB R1, R2, R3`                   :R1=R2-R3  
(R1 contains the result of subtracting the contents of R2 and R3)
  - `XOR R1, R2, R3`                   :R1=R2 xor R3  
(R1 contains the result of bitwise exclusive-OR-ing the contents of R2 and R3)

Assume that registers A and B have arbitrary contents. What are the results of the following sequences of operations:

1. `SUB A, A, B`  
   `ADD B, B, A`  
   `SUB A, B, A`
2. `XOR B, B, A`  
   `XOR A, A, B`  
   `XOR B, B, A`

**Q7- Processing unit [17 marks]**

- a) Assume that a program P takes 10 seconds to run on a 100MHz CPU A
  - What clock speed would be required for a CPU B to execute P in 8 seconds, assuming that P uses the same number of clock cycles on B as on A? (You may assume that memory access cycle will also be faster)
  - What clock speed would be required for a CPU C to execute P in 6 seconds, assuming that P requires 20% more clock cycles on CPU C?
- b) Define the concept of instruction pipelining. Assume that there is a three-stage instruction pipeline (fetch-decode, execute). Draw the timing diagram to show how many time units are needed for execution of three instructions.
- c) A computer with a five-stage pipeline deals with conditional branches by stalling for the next three cycles after hitting one. How much does stalling hurt the performance if 20% of all instructions are conditional branches? Ignore all sources of stalling except conditional branches.