

National Exams – December 2003

98-Elec-A4, Digital Systems and Computers

3 Hours Duration

NOTES

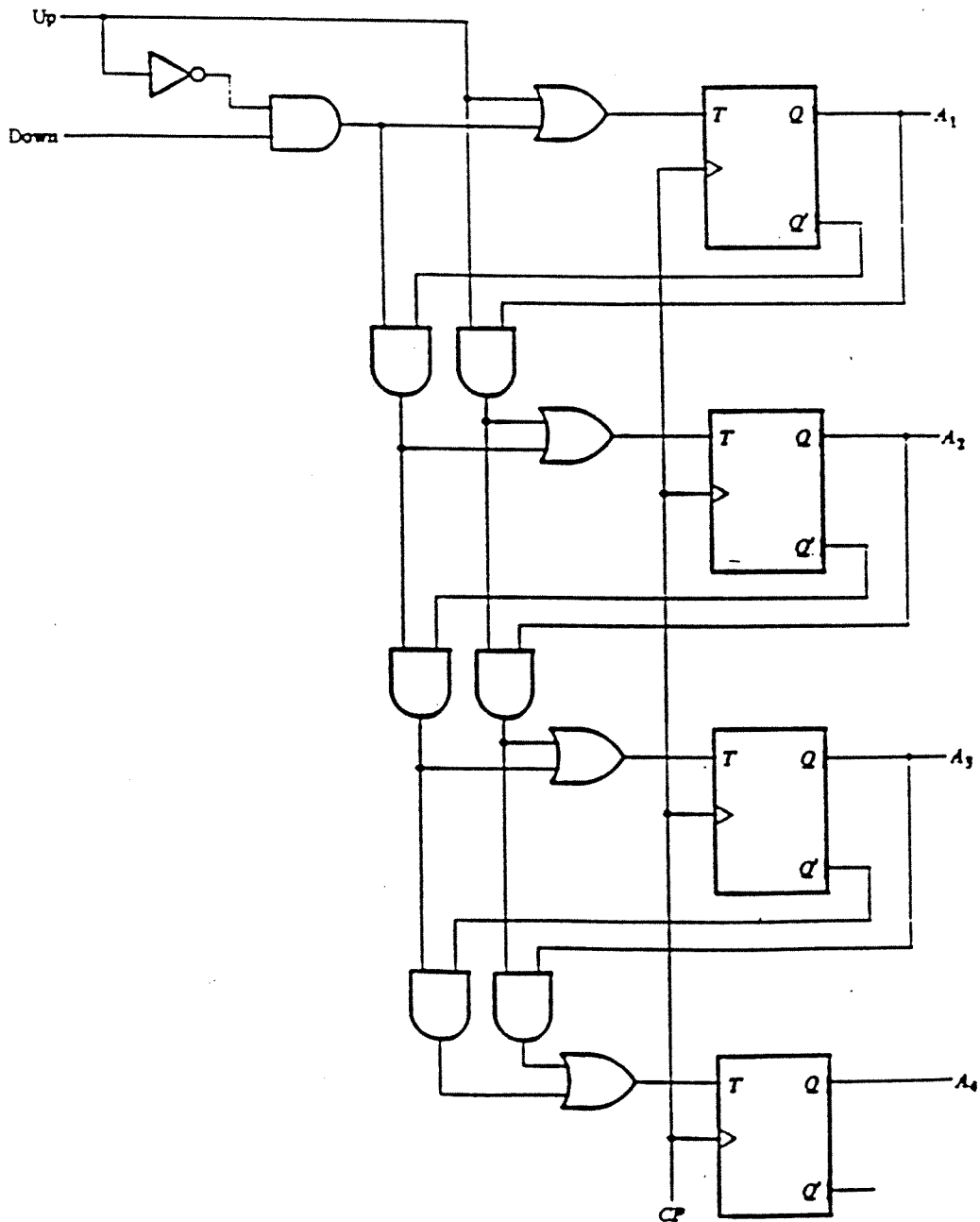
1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made.
2. Candidates may use one of two calculators, the Casio or Sharp approved models. This is a Closed Book exam.
3. Any five questions constitute a complete paper. Only the first five questions as they appear in your answer book will be marked.
4. All questions are of equal value.

1. Simplify the following Boolean function F together with the don't-care conditions d. (a) Determine the prime implicants of F using Karnaugh Mapping techniques. (b) Draw the combinational logic circuit which implements F.

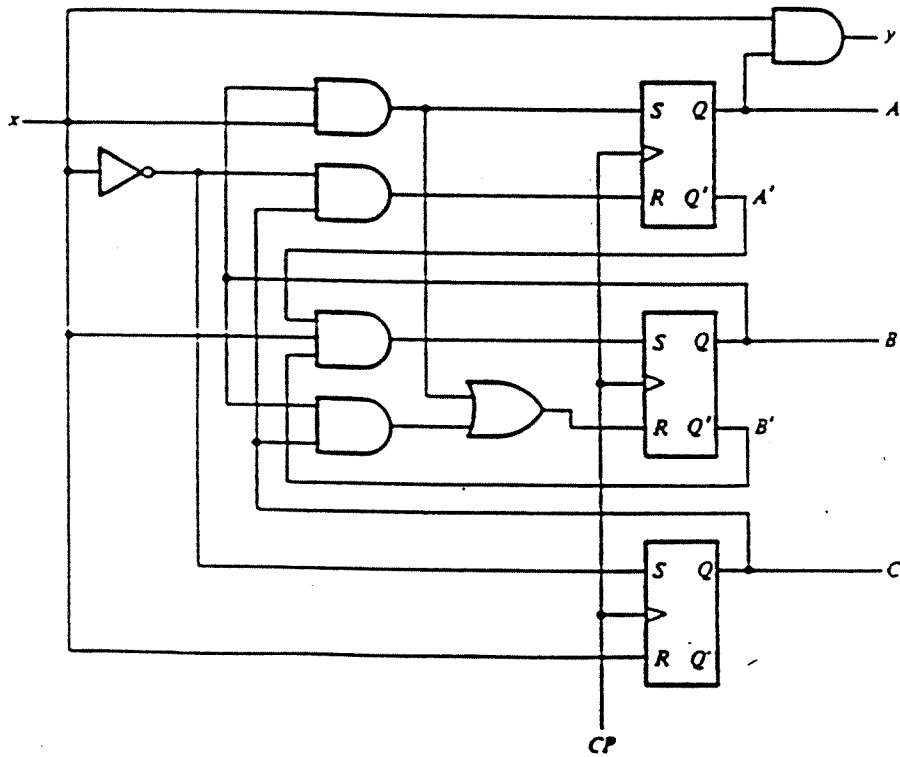
$$F(A, B, C, D) = \Sigma(1, 3, 5, 7, 9, 15)$$

$$d(A, B, C, D) = \Sigma(4, 6, 12, 13)$$

2. The circuit shown below is a synchronous up-down counter.
- Derive the expressions for the T inputs of each flip-flop for the up-mode and the down-mode.
 - What happens if the up and down inputs are both 0?
 - What happens if the up and down inputs are both 1?
 - Why is the circuit referred to as synchronous, rather than asynchronous?
 - What is the mod. of this counter?



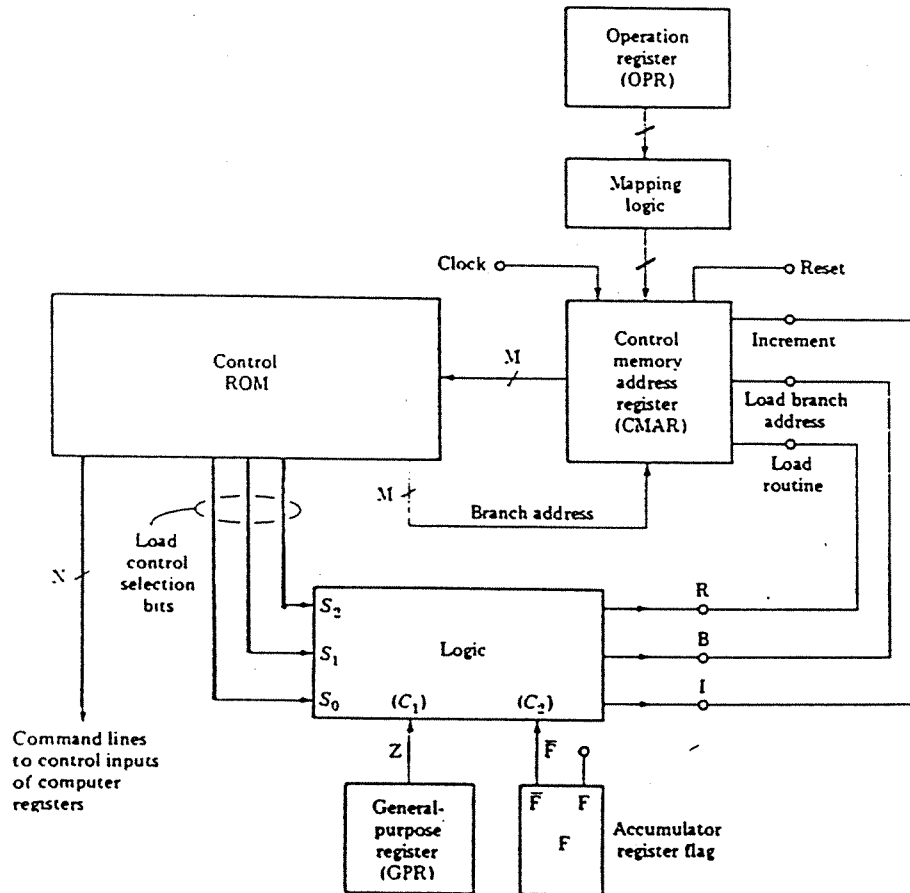
3. The following digital circuit has been designed by someone and you are asked to produce the state diagram for the circuit. It is known that three of the states (i.e.: 000, 110 and 111) are not used by the circuit. Draw the state diagram and demonstrate that if the state 110 is encountered due to electrical noise, that the circuit will return to used states after one or two clock cycles.



4. Write short paragraphs (approximately 200 words) on the operation of each of the following kinds of MOS memories.
- a) Sequentially accessed (FILO and FIFO).
 - b) Random accessed (RAM), and
 - c) Read only (ROM), including EEPROM.

Illustrate your description with logic circuits as well as with integrated circuits. Comment on addressing, programming and erasing times, memory capacity, and cost. Describe the difference between static and dynamic memory and also indicate when and how one would use the three types of memories listed above.

5. The following architecture represents a ROM controller for a microcomputer. The logic box in the controller with inputs S_2, S_1 and S_0 (load control selection bits) and C_1, C_2 (status bits), has to be designed using combinational logic gates. Considering that the truth table for this logic box is given at the bottom of the circuit, draw the minimum circuit necessary to implement the truth table.



S_2	S_1	S_0	C_1	C_2	B	I	R
0	0	1	X	X	0	0	1
0	1	0	X	X	0	1	0
0	1	1	0	X	1	0	0
1	0	0	1	X	1	0	0
1	0	1	X	0	0	1	0
1	1	0	X	1	0	0	1
0	1	1	1	X	0	1	0

