

**National Exams December, 2004****98-Comp-A2/Soft-A2  
Digital Systems Design****3 hours duration****NOTES:**

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper a clear statement of any assumptions made.
2. This is an OPEN BOOK exam. No calculators are permitted.
3. Any FOUR (4) questions constitute a complete paper. Only the first four questions as they appear in your answer book will be marked.
4. Each question is of equal value. Marks for multipart questions are stated in each part.

**Question 1 (25 Marks)**

A particular system has three input bits designated X1, X2 and X3, and two outputs, designated Y1 and Y2. The system is to do the following:

Y1 will be high if and only if X1:X2:X3 are 110 respectively and the immediately previous values of X1:X2:X3 were 010. Y2 will be high if X1:X2:X3 are 01x and the immediately previous values of X1:X2:X3 were x01, respectively, and the previous Y1 = 0 and its value two times previously is Y1 = 1. Note that 'x' indicates 'don't care'.

For example, the following sequence of inputs will yield the corresponding outputs. Note that the bits to the left are the oldest bits, the bits on the right are the most recent. The rightmost column contains the current signals.

X1	1 0 1 1 0 1 0 1 1 0 0 0 1 0 0 1 0 0 1 1 0 0 0 0 0 1 0 1 0 1
X2	0 0 0 1 1 0 0 1 0 1 0 1 1 0 1 0 0 1 1 0 1 0 0 1 0 1 0 0 1 0
X3	0 0 0 1 0 1 0 0 1 1 0 0 0 1 1 0 1 0 0 1 1 1 0 0 1 0 0 0 0 0
Y1	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0
Y2	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0
oldest	most recent

Design the system. Try to minimize the number of states used and the number of gates and flip-flops. Use D flip-flops.

**Question 2 (25 Marks)**

a) (10 Marks) The specifications for standard logic families define set-up and hold times. What are these times? For what kind of circuits do these times apply? What might happen if these times are not met? When reading a specification sheet, the set-up and hold times are listed as maximum times. How does the circuit designer use this information in his/her design? What range of set-up time must your design provide to ensure that a device with a specified maximum set-up time of 10 nS works properly?

b) (15 Marks) Binary counters and shift registers can have more than one output change state at every clock pulse. Sometimes the outputs of these counters are combined through combinatorial logic gates and used to trigger external events. What problems can occur due to set-up time, hold time and propagation time considerations? Answer this question by making specific reference to the circuit of Figure 1.

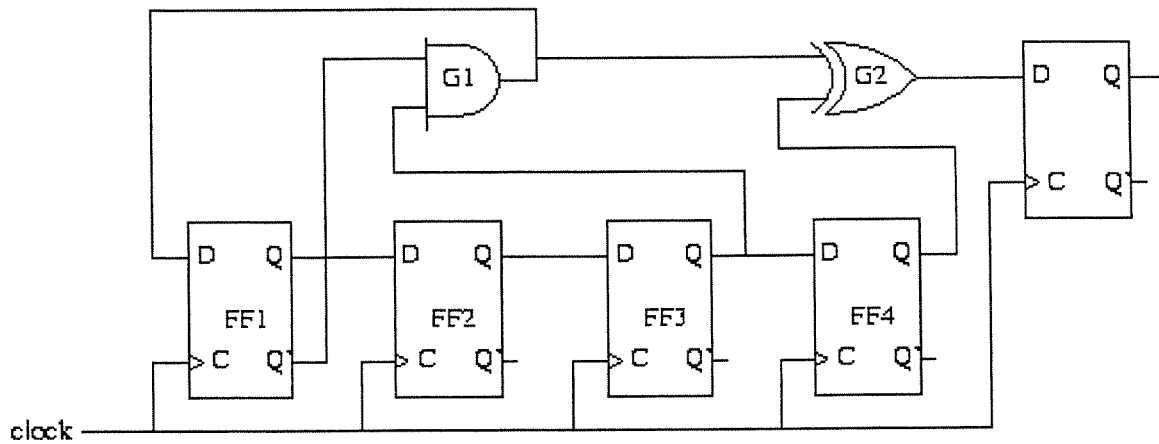


Figure 1: Circuit for part b) of Question 2.

**Question 3 (25 Marks)**

a) **(15 Marks)** Sketch the data path internal to the CPU for a microprocessor with which you are familiar and describe the cycle-by-cycle flow of signals in the datapath. Your description should commence at the point where the processor is starting to read the next instruction and should end when the processor is about to read the subsequent instruction. Use a table in your explanation, with each row down the table as the next clock “tick”

b) **(5 Marks)** When an interrupt occurs during the execution of a program, what happens? Briefly discuss what happens cycle-by-cycle for a particular processor with which you are acquainted. The discussion should start with the instruction that gets interrupted and continue through to the start of the execution of the first part of the first instruction in the Interrupt Service Routine. Assume that this is a hardware-vectorred interrupt.

c) **(5 Marks)** Key issues that must be addressed in the design of a system with multiple interrupt sources include the length of the interrupt service routines, latency and nesting. Briefly explain each issue and why it is important.

**Question 4 (25 Marks)**

a) **(15 Marks)** When passing data from one computer system to another, it is especially important that each unit of information is exchanged properly. Consider the case where the transmitting computer outputs 100 kilobytes/second on a parallel port, but the receiver can read only 50 kilobytes/second on the port. Clearly, every second byte is lost. Assuming that we cannot speed up the receiver nor slow down the transmitter, what signals can we add to the interface, in what direction do they go (from transmitter to receiver or vice versa) and how do we control or use them so that we can guarantee that

every byte will be read once and once only. Note that your answer should still work if the transmitter is slower than the receiver.

b) **(10 Marks)** Why is it possible to transfer data synchronously so much faster than asynchronously? Your answer should convey your understanding of the essential issues in both techniques.

### **Question 5 (25 Marks)**

a) **(10 Marks)** An embedded system (a microprocessor system) is being designed to have a 24-bit address bus with a linear address range. The memory is not organized in banks. The system must have ROM from addresses \$d00000 to \$ffffff, RAM from \$000000 to \$00ffff, and four I/O devices occupying 16 bytes each anywhere in the address range from \$100000 to \$17ffff. The system will never be expanded.

The ROM is made up of devices that store 512 KBytes x 8-bits each, the RAM consists of parts that store 128 Kbytes each, and the I/O devices occupy 16 consecutive bytes each.

Design an address decoder for this system. Use as few gates as possible. Note that all devices use active low chip select inputs.

b) **(10 Marks)** A typical microprocessor has a bus architecture. There are two often-used bus structures. These are the von Neumann architecture and the Harvard architecture. Briefly describe each of these and suggest the strengths and weaknesses of each.

c) **(5 Marks)** What must a microprocessor do when the RESET input to it is changed from the asserted state to the de-asserted state? Discuss all of the steps at a high level of detail.