

National Exams May 2013

07-Elec-A4, Digital Systems & Computers

3 hours duration

NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to submit with the answer paper, a clear statement of any assumptions made.
2. This is a Closed Book exam.
Candidates may use one of two calculators, the Casio or Sharp approved models.
3. FIVE (5) questions constitute a complete exam.
Clearly indicate your choice of any five of the six questions given otherwise the first five answers found will be considered your pick.
4. All questions are worth 12 points.
See below for a detailed breakdown of the marking.

Marking Scheme

1. (a) 2, (b) 2, (c) 2, (d) 3, (e) 3, total = 12
2. (a) 2, (b) 4, (c) 2, (d) 4, total = 12
3. (a) 3, (b) 3, (c) 3, (d) 3, total = 12
4. (a) 3, (b) 3, (c) 6, total = 12
5. (a) 4, (b) 4, (c) 4, total = 12
6. (a) 2, (b) 3, (c) i. 3, (c) ii. 2, (c) iii. 2, total = 12

The number beside each part above indicates the points that part is worth

- 1.- A combinational circuit taking a nonnegative three digit binary number ABC as input decides whether it is an even number or the two most significant digits A & B are equal (indicating it with output E = 1) and whether the sum of its two least significant digits B & C is odd (indicating it with output O = 1).
- Provide the truth table for the circuit.
 - Write output E in canonical sum-of-products (SoP) form.
 - Write output O in canonical product-of-sums (PoS) form.
 - Use Boolean identities to find the minimized SoP form for output E.
 - Use Boolean identities to find the minimized PoS form for output O.

Note: Please find a table with Boolean identities attached in the last page

- 2.- (a) Provide the state transition table for an asynchronous binary up-counter that will go through the sequence 0000, 0001, 0010, ..., 1111, 0000,
- Build the asynchronous binary up-counter in (a) using T flip-flops.
 - Provide the state transition table for a decade counter.
 - Build an asynchronous decade binary up-counter using T flip-flops.

Hint: Try modifying the counter in (b) such that it turns into a decade counter.

- 3.- Use JK flip-flops to design a finite state machine (FSM) that works as a 2-bit binary synchronous up-counter when its input X = 0 and as a 2-bit binary synchronous down-counter when its input X = 1.
- Draw the state transition diagram.
 - Build the state transition table. Include values of flip-flop inputs.
 - Find minimized logic expressions for flip-flop inputs.
 - Draw the resulting logic circuit that implements this FSM.

Note: Please find flip-flop excitation tables attached in the last page

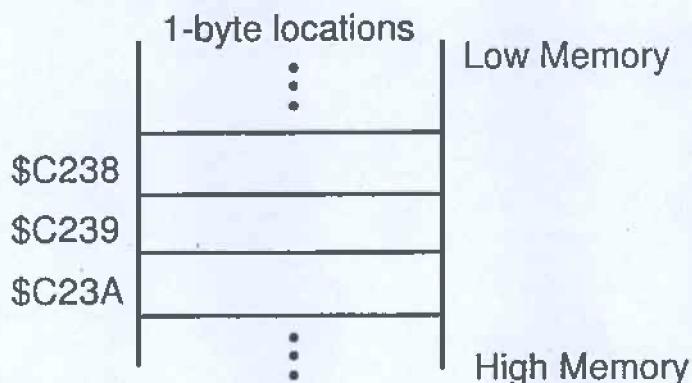
- 4.- (a) Where is the use of a parallel-to-serial shift register needed, in the receiving unit of a serial communication port or in its transmitting unit? Explain.
- (b) Where is the use of a serial-to-parallel shift register needed, in the receiving unit of a serial communication port or in its transmitting unit? Explain.
- (c) Draw the circuit for a 4-bit shift register using D flip-flops that can perform parallel-to-serial conversion as well as serial-to-parallel conversion.

In your diagram, identify:

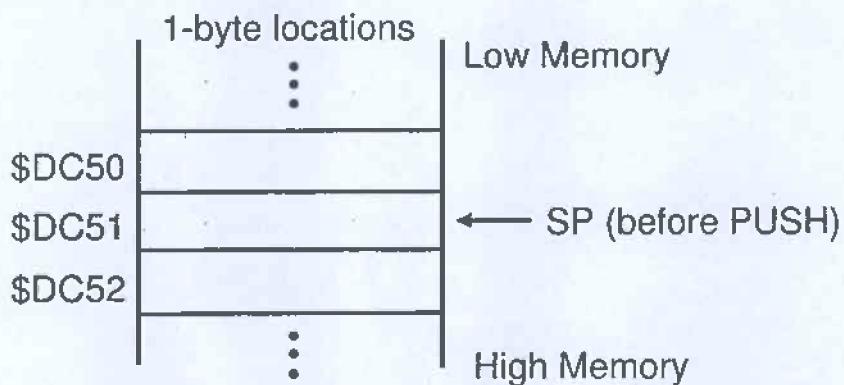
- The serial input terminal,
- The serial output terminal,
- The parallel input terminals, and
- The parallel output terminals.

- 5.- For microprocessors, such as Motorola's, that use big-endian order for storing multiple-byte variables

- (a) Fill the memory block below with the result of the instruction:
"Store the 16-bit number \$7A01 to address \$C239"



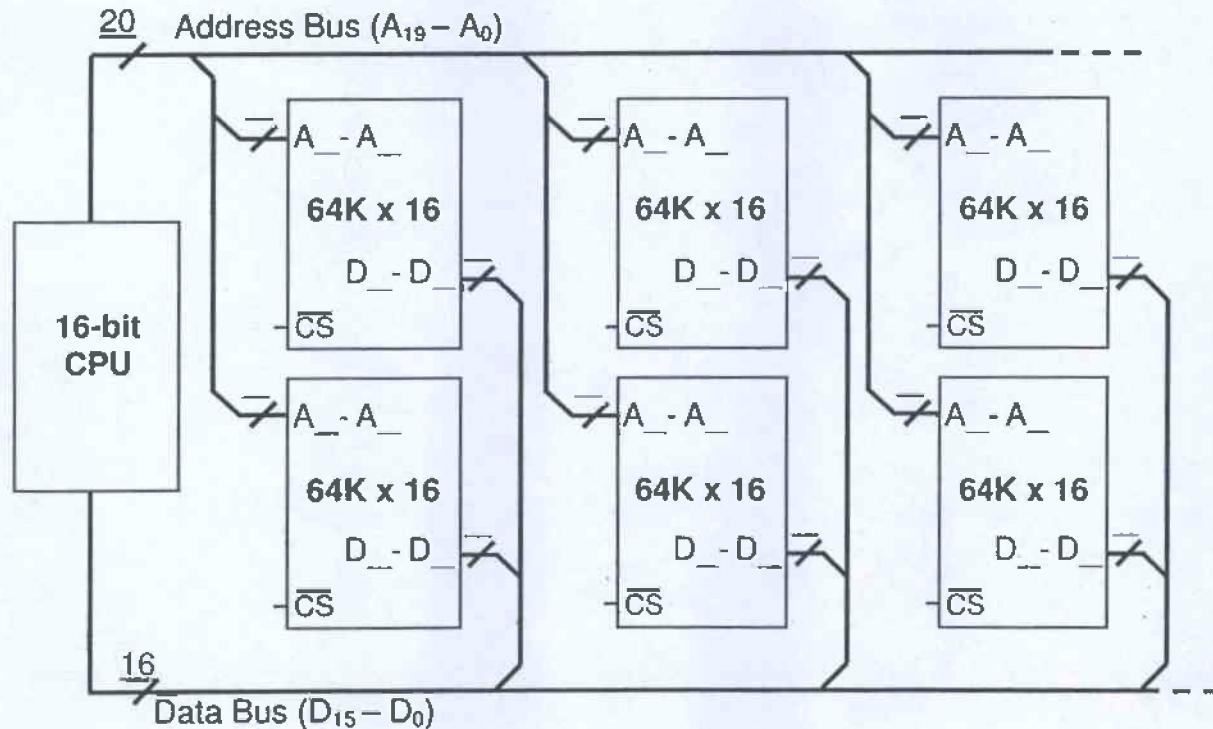
- (b) Let SP = \$DC51. Fill the memory block below with the result of the instruction:
"Push the 16-bit number \$7A01 onto the stack"



- (c) What is the value of the stack pointer register SP after the PUSH?

- 6.- (a) Mention two differences between the address bus and the data bus of a computer system in terms of the direction information can flow in them and the meaning of the information each carries.
- (b) A microprocessor system has an address bus with 20 lines, $A_{19}-A_0$, and a data bus with 16 lines, $D_{15}-D_0$. What is the memory space of the system (in KByte and MByte)? Justify. Indicate the address range of the entire memory space providing the lowest and highest addresses in hexadecimal.
- (c) Provide the 16-bit CPU in the figure below with a 512KByte memory space by making use of $64K \times 16$ memory chips like the ones provided in the figure below.
- How many chips are needed?
Fill in the blanks *beside* and *inside* the memory chips with the appropriate numbers.
The number on top of this symbol represents the number of lines on that bus. The spaces besides the A's and the D's indicate which set of lines of the address or data bus is connected to each chip, respectively.
 - Complete the connections in the figure below adding logic gates where needed to produce the chip select (CS) signals needed (the decoding logic). Explain the reasons for the connections made; include expressions for the Boolean logic used.
 - Provide the address range allocated to each chip in hexadecimal.

Note: R/W & clock signals are omitted for simplicity.



Excitation Table

Q	Q+	R	S	J	K	T	D	:
0	0	X	0	0	X	0	0	
0	1	0	1	1	X	1	1	
1	0	1	0	X	1	1	0	
1	1	0	- X	X	0	0	1	

Basic Boolean Identities

Identity	Comments
1. $A + 0 = A$	Operations with 0 and 1
2. $A + 1 = 1$	Operations with 0 and 1
3. $A + A = A$	Idempotent
4. $A + \bar{A} = 1$	Complementarity
5. $A \cdot 0 = 0$	Operations with 0 and 1
6. $A \cdot 1 = A$	Operations with 0 and 1
7. $A \cdot A = A$	Idempotent
8. $A \cdot \bar{A} = 0$	Complementarity
9. $\bar{\bar{A}} = A$	Involution
10. $A + B = B + A$	Commutative
11. $A \cdot B = B \cdot A$	Commutative
12. $A + (B + C) = (A + B) + C = A + B + C$	Associative
13. $A \cdot (B \cdot C) = (A \cdot B) \cdot C = A \cdot B \cdot C$	Associative
14. $A \cdot (B + C) = (A \cdot B) + (A \cdot C)$	Distributive
15. $A + (B \cdot C) = (A + B) \cdot (A + C)$	Distributive
16. $A + (A \cdot B) = A$	Absorption
17. $A \cdot (A + B) = A$	Absorption
18. $(A \cdot B) + (\bar{A} \cdot C) + (B \cdot C) = (A \cdot B) + (\bar{A} \cdot C)$	Consensus
19. $\overline{A + B + C + \dots} = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \dots$	De Morgan
20. $\overline{A \cdot B \cdot C \cdot \dots} = \bar{A} + \bar{B} + \bar{C} + \dots$	De Morgan
21. $(A + \bar{B}) \cdot B = A \cdot B$	Simplification
22. $(A \cdot \bar{B}) + B = A + B$	Simplification