# National Exams May 2015 

98-Comp-A1, Electronics

3 hours duration

## NOTES:

1. If doubt exists as to the interpretation of any question, the candidate is urged to indicate, with the answer, a clear statement of any assumptions made.
2. This is a OPEN BOOK exam.

Any non-communicating calculator is permitted.
3. FIVE (5) questions constitute a complete exam paper.

The first 5 questions as they appear in the answer book will be marked.
4. Each question is of equal value.

## Question 1 (20 marks)



Figure 1. The diodes have a voltage drop $\mathrm{V}_{\mathrm{D}}=0.7 \mathrm{~V}$ in forward bias.
For the circuit shown in Figure 1:
a) Sketch $V_{i}$ and $V_{o}$ as a function of time, indicating peak voltages.
b) How should $D_{1}$ be rated for power consumption?
c) What is the peak current in $R_{1}$ ?


Figure 2. The diodes have a voltage drop $\mathrm{V}_{\mathrm{D}}=0.7 \mathrm{~V}$ in forward bias.
For the circuit shown in Figure 2:
d) ) Sketch the output waveform $V_{o}(t)$ in steady state. Label key voltages and times, and indicate changes in operating region for the diodes.

## Question 2 (20 marks)



Figure 3. $\mathrm{k}_{\mathrm{n}}{ }^{\prime}=\mu_{\mathrm{n}} \mathrm{C}_{\mathrm{ox}}=1 \mathrm{~mA} / \mathrm{V}^{2}, \mathrm{~W} / \mathrm{L}=10, \mathrm{~V}_{\mathrm{tn}}=1 \mathrm{~V},\left|\mathrm{~V}_{\mathrm{A}}\right|=100 \mathrm{~V}$
For the circuit shown in Figure 3:
a) For $\mathrm{Vi}=2 \mathrm{~V}$ what is the current through Q 3 ?
b) What is $V_{D S}$ for Q1?
c) Draw a small signal equivalent model for the circuit.
d) What is the small signal AC gain of the circuit?

## Question 3 (20 marks)



Figure 4.
For the circuit shown in Figure 4:
a) Derive the transfer function $\frac{V o(j \omega)}{V i(j \omega)}$ for the circuit shown in Figure 4, assuming the op-amp is ideal.
b) Sketch the frequency response, indicating the 3 dB frequency for this circuit.
c) If $V_{i}(t)=10 \sin (120 \pi \mathrm{t}) \mathrm{V}$, find $V_{o}(j \omega)$.
d) If $V_{i}(t)=10 \sin (120 \pi \mathrm{t}) \mathrm{V}$, find $V_{o}(t)$.

## Question 4(20 marks)



Figure 5. $\mathrm{V}_{\mathrm{be}}=0.7 \mathrm{~V}$ (active), $\mathrm{V}_{\mathrm{ce}}=0.2 \mathrm{~V}$ (saturation), $\beta=100$.
For the circuit shown in Figure 5:
a) If $V_{i}=0 V D C$, find the DC bias point for Q1?
b) Draw the small signal equivalent circuit and evaluate the small signal AC voltage gain.
c) Sketch $I_{c}$ vs $V_{c e}$ and show the operating point for the transistor.
d) How would you change the bias to obtain maximum signal swing?

## Question 5 (20 marks)



Figure 6. Assume the gates are ideal and switch at $\mathrm{V}_{\mathrm{DD}} / 2$.
For the circuit shown in Figure 6:
a) Explain the operation of this circuit.
b) Sketch the waveforms $V_{c}(t)$ and $V_{\text {out }}(t)$.
c) Find an expression for $V_{c}(t)$.
d) Find the period of the waveform if $R_{1}=10 \mathrm{k} \Omega$ and $C_{1}=10 \mathrm{nF}$.

## Question 6 (20 marks)



Figure 7. $\mathrm{k}_{\mathrm{n}}{ }^{\prime}=50 \mu \mathrm{~A} / \mathrm{V}^{2}, \mathrm{k}_{\mathrm{p}}{ }^{\prime}=20 \mu \mathrm{~A} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{tn}}=-\mathrm{V}_{\mathrm{tp}}=1 \mathrm{~V}, \mathrm{C}_{\mathrm{ox}}=1 \mathrm{fF} / \mu \mathrm{m}^{2}, \mathrm{~V}_{\mathrm{DD}}=5 \mathrm{~V}$.
a) If the minimum gate length for this technology is $1 \mu \mathrm{~m}$, size $\mathrm{Q}_{\mathrm{N}}$ and $\mathrm{Qp}_{\mathrm{p}}$ to obtain a symmetric transfer characteristic.
b) Estimate the maximum capacitance this circuit can drive with a propagation delay of less than 200 ps .


Figure 8.
For the circuit shown in Figure 8:
c) Determine outputs X and Y for all possible inputs A and $\mathrm{B} . \phi$ is a clock signal.
d) If $Q_{1}$ and $Q_{2}$ are sized as in part a), find a minimum size for $Q_{5}$ and $Q_{6}$ that will ensure X can be pulled down to $\mathrm{V}_{\mathrm{DD}} / 2$ or lower.

## Question 7 (20 marks)



Figure 9.
a) What is a common name for the ADC circuit shown in Figure 9? What is a principal advantage of this circuit over other ADC implementations?
b) What are the analog voltages at each of the comparator negative inputs? If $V_{\text {in }}=3 \mathrm{~V}$ what are the logic values for $V_{1}$ through $V_{4}$ ?
c) List all possible combinations of $\mathrm{V}_{1}-\mathrm{V}_{4}$ and the corresponding binary output.
d) In an integrated circuit, how could $V_{\text {ref }}$ be generated?

## Marking Scheme

1. 20 marks total (4 parts, 5 marks each)
2. 20 marks total ( 4 parts, 5 marks each)
3. 20 marks total (4 parts, 5 marks each)
4. 20 marks total (4 parts, 5 marks each)
5. 20 marks total (4 parts, 5 marks each)
6. 20 marks total (4 parts, 5 marks each)
7. 20 marks total (4 parts, 5 marks each)
